A SURVEY OF ANALOG FUNCTION AND ANALOG INTERFACING DEVICES

Marcelo Ozorio Rosa

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NAVAL POSTGRADUATE SCHOOL

Monterey, California

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A Survey of Analog Function and

Analog Interfacing Devices

by

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A survey has been made of analog IC circuits based on manufacturers specifications. The survey considers analog multipliers, log amplifiers, charge-transfer devices, sample-holds, A/D and D/A converters, and an analysis of device parameters to derive a uniform set of descriptors has been accomplished. Substantially, all devices currently available have been catalogued using these uniform descriptors. Sufficient descriptive and tutorial material is also included to allow use of the catalog as a selection guide. Based on this survey, analog IC building blocks are readily available and the applicatio

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A Survey of Analog Function and Analog Interfacing Devices

by

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ABSTRACT

A survey has been made of analog IC circuits, based on manufacturers specifications. The survey considers analog multipliers, log amplifiers, charge-transfer devices, sample-holds, A/D and D/A converters, and an analysis of device parameters to derive a uniform set of descriptors has been accomplished. Substantially, all devices currently available have been catalogued using these uniform descriptors. Sufficient descriptive and tutorial material is also included to allow use of the catalog as a selection guide. Based on this survey, analog IC building blocks are readily available and the application potential is very great.

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I. INTRODUCTION

During the past few years, a growing design sophistication has been in evidence at the linear IC manufacturing field. With diminishing new-product opportunities for amplifier circuits and increasing IC technological know-how linear IC manufacturers are now realizing complete circuit functions on a single chip - multipliers, dividers, log amps and waveform generators, to name but a few. Ultimately, the specialized complete-function chips will replace the amplifier chips in many situations and may eventually flatten the growth of the amplifier production, perhaps like the wide variety of available IC amplifiers affected the growth of the transistor business.

The impact of the technological strides being made in linear IC technology has been felt also in the area of Analog/Digital interfacing. A new generation of A/D and D/A converter circuits employing IC technology is now beginning to appear with advantages in high packing density and low cost.

In the signal processing field, Charge-Transfer Devices experienced a huge diversification in manufacture and application technology since their announcement a few years ago. From the initial effort on light-imaging arrays, a capability has evolved for performing other functions in the computer and analog signal processing areas which may ultimately have a far greater impact. Charge-transfer devices methods of handling analog signals permit addition and multiplication to be performed directly without A/D conversion and high-speed computer utilization, thereby providing orders of magnitude

reductions in size, weight and cost. Applications for such techniques abound throughout the communications, navigation, radar and sonar fields.

Because of the variety of devices and lack of standardization of specifications, it is difficult to compare the suitability of commercially available devices for a particular application using only the manufacturer's literature.

A survey and analysis have been made of analog IC circuits. The purpose was to identify the availability of analog IC building blocks, their applications and current state-of-the-art. The survey considered analog multipliers, log amplifiers, charge-transfer devices, sample-holds, A/D and D/A converters. In each category, design techniques, applications and state-of-the-art were identified and analyzed, based on manufacturer specifications. It was necessary to generate a standardized set of descriptors for each type of device, to which the manufacturers specifications could be translated. Data thus translated have been organized in tabular form for ease of application to any given design problem. From this survey it appears that analog IC building blocks are readily available and the application potential is very great. However, information concerning charge-transfer device applications needs to be augmented by definitive knowledge of actual performance in signal processing systems.

II. ANALOG MULTIPLIERS

A. GENERAL DESCRIPTION

In a variety of circuit or system applications, it is necessary to obtain an analog output signal which is a linear product of two input signals. The circuit block which can perform this function is the analog multiplier. In such a circuit block, the output voltage Z must be proportional to the product of the two inputs, X and Y, i.e.,

$$Z = K.X.Y \qquad (1)$$

where K is the gain constant of the multiplier. In most applications it is also required that the output Z must conserve the polarity relationship between the two inputs such that each of the inputs can either be positive or negative, and the output would be of the polarity implied by Eq. (1). A multiplier which has this property is called a "four-quadrant multiplier".

Some of the most common parameters used in describing the performance of a four-quadrant multiplier are the accuracy, output offset, bandwidth, temperature stability, and slew rate. Each of these parameters can be briefly defined as follows:

Accuracy is the maximum deviation of the actual output level from the ideal one, for any choice of X or Y values within the dynamic range of the multiplier. It is normally specified as a percentage of full scale output.

Output offset is defined as the output voltage observed when $X = Y = 0$.

Bandwidth describes the high frequency capabilities of an analog

multiplier. Small-signal 3 db bandwith is the frequency at which the output is 3 db down from its low frequency value, for a constant input level.

Temperature stability is normally measured in terms of the temperature drift of the output offset and full-scale accuracy.

Slew rate is the time rate of change of the output voltage, for a voltage step applied at the input.

B. APPLICATIONS

The analog multiplier forms a versatile building block for performing a number of mathematical operations such as multiplying, dividing, squaring, and square-root extraction. In most of these applications, it is used in conjunction with an operational amplifier to complement its functional capability. Figure 1 outlines some of the applications of an analog multiplier in accomplishing basic mathematical operations.

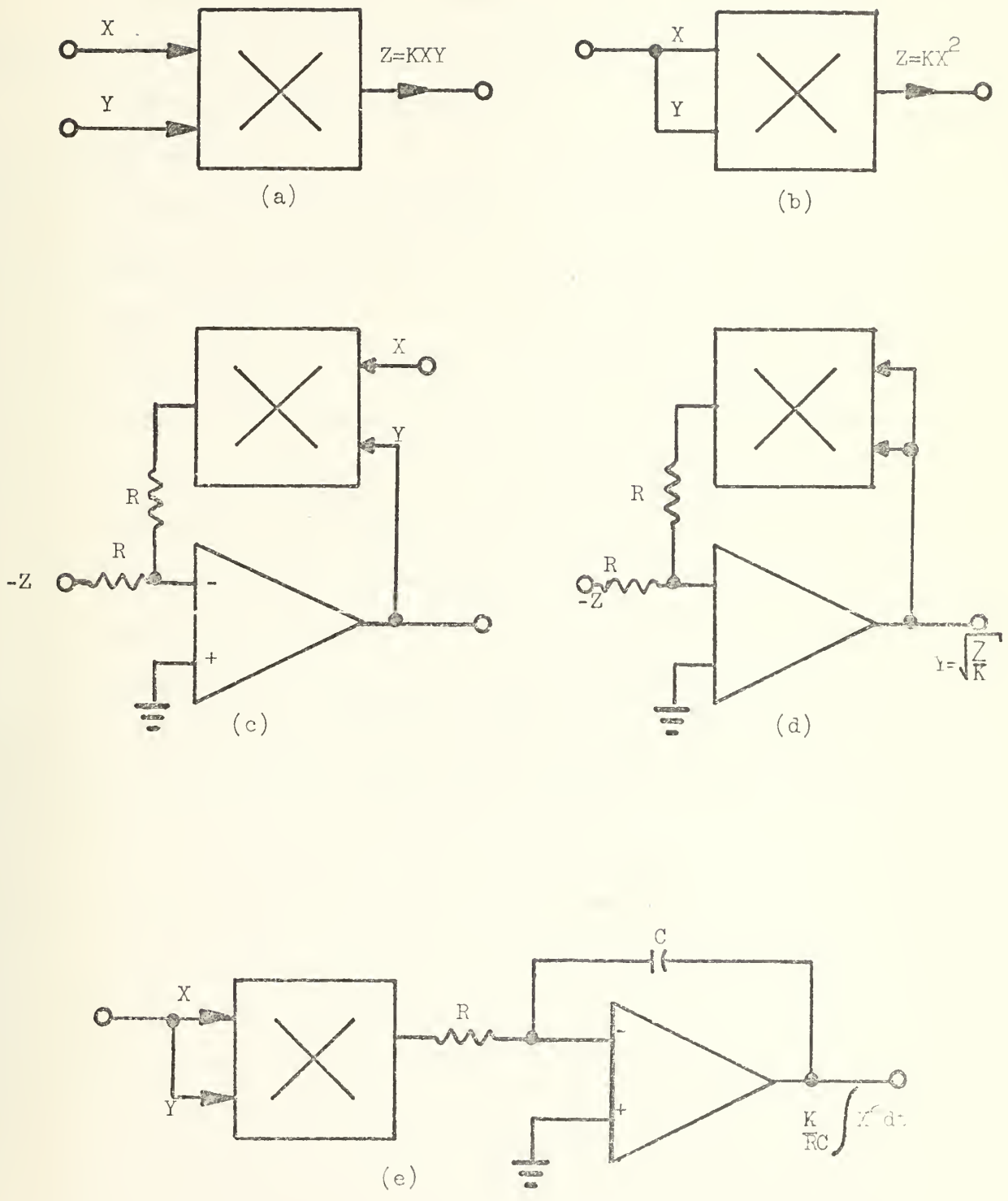

Figure 1. Some basic applications of an analog multiplier: (a) Multiplication, (b) squaring, (c) division, (d) square root, (e) mean square

In addition to performing mathematical operations, analog multipliers can be utilized to develop the following circuit functions:

1. Suppressed Carrier AM Modulation
2. AGC Circuits
3. Synchronous AM and FM Detection
4. Frequency Multiplication
5. Phase Detection
6. Video Detection
7. TV Color Chroma Demodulation
8. FM Stereo Decoding
9. Sample and Hold Circuits
10. Voltage-Controlled Oscillators
11. Phase Locked Loops

In each particular application, there are usually a dominant parameter and a second parameter which influence multiplier choice. A selection guide for multipliers by key parameter is given in Table I.

Table I - Multipliers Application Guide By Key Feature

KEY FEATURE	MULTIPLIER APPLICATION
High precision, low noise and drift	Analog computation, dividers, servo multipliers, correlators
Low Drift, good accuracy, lower cost	Wide temperature range, general purpose multiply/divide
Bandwidth, accuracy	Graphic displays, dividers
Wide dynamic divide range, accuracy	Root and power generation
External trim for accuracy	R and D, medical, laboratory, analog computation
Economy, size	OEM designs, general purpose multiply/divide
MIL spec. available	Military grade design

C. CIRCUIT TECHNIQUES

There are several circuit methods which can be applied in generating an output proportional to the product of two input signals. The major techniques in today's solid state multipliers can be classified into two categories: variable transconductance and pulse-width/amplitude modulation.[1]

1. Variable-Transconductance Multipliers

The variable-transconductance method makes use of the dependence

1. Historically, the first process of analog multiplication was the piecewise-linear approximation (quarter square) scheme, using diode shaping techniques to form the square of the sum and the difference of the two input voltages, followed by the triangle averaging method; both designs can be said as approaching obsolescence.

of the transistor transconductance on the emitter current bias. These multipliers have good accuracy and bandwidth, are low in cost and well suited to most applications unless extreme stability over wide temperature range is required. The linearized transconductance principle is a new development in this technique, increasing substantially the accuracy of monolithic multipliers.

2. Pulse-Width/Amplitude Modulation Multipliers

In the pulse-width/amplitude modulation method, the output is the average value of a pulse modulated in amplitude by the first input signal, and modulated in width by the second one. This technique provides very high accuracy and stability, at reasonable speed. While not as low in cost as the transconductance type, it is superior for applications demanding the best accuracy attainable, over a wide temperature variation.

A comparison of these alternate techniques is given in Table II, describing their present-day capabilities in key performance areas - accuracy, stability, bandwidth and slew rate.

Table II

Comparative Characteristics of Multiplier Types and Classes (Typical Values)

Type	Performance Class	Accuracy % of F.S. (±)	Accuracy Stability % of F.S./°C	Offset Stability mv/°C	Bandwidth (-3db, Small Signal) kHz	Slew Rate V/usec
Variable Transconductance	Moderate Accuracy and Bandwidth	1 to 2	0.03 to 0.06	0.4 to 3	300 to 1,000	2 to 45
	High Accuracy, Moderate Bandwidth	0.2 to 0.5	0.01 to 0.02	0.2 to 1	300 to 1,000	3 to 6
	Moderate to High Accuracy, Wideband	0.5 to 2	0.01 to 0.06	0.2 to 2	1,000	25 to 55
	High Accuracy, Wideband	0.5 to 1	0.02 to 0.05	1 to 2	2,500 to 10,000	100 to 150
Pulse-Width/ Amplitude Modulation	High Accuracy, Moderate Bandwidth	0.1 to 0.25	0.01 to 0.02	0.25	7 to 100	0.3 to 3

D. STATE-OF-THE-ART

1. Performance

Table III lists the current state-of-the-art in five most significant specifications of analog multipliers, also tabulating the associated circuit technique.

Table III

State-of-the-Art in Analog Multipliers (best values)

Specification	Performance	Method
Accuracy	0.1% F.S.	Pulse-Width/Amplitude Modulation
Accuracy Drift	0.01%/°C	Pulse-Width/Amplitude Modulation, Variable-Transconductance
Offset Drift	0.2 mV/°C	Variable Transconductance, Linearized Transconductance
-3 db Small-Signal Bandwidth	10 MHz	Variable Transconductance
Slew Rate	150 V/usec	Variable Transconductance

2. Technology

Modular construction is presently used in variable-transconductance and pulse-width/amplitude modulation multipliers.

Monolithic analog multipliers currently available use the linearized transconductance technique, which can produce full-scale accuracy

of 0.2% to 0.3%, mainly by careful transistor matching. They also have greater bandwidth and lower cost than discrete multipliers using the pulsewidth/amplitude modulation technique, which achieve 0.1% F.S. accuracy. A Monolithic PWAM multiplier was recently[2] demonstrated which requires external capacitor and low pass filter, achieving accuracies better than 0.5% without trimming. Temperature stability is typically 0.005%/°C.

A recent development in monolithic multipliers technology utilizes active-operation laser trimming of thin-film resistors deposited on the monolithic chip, eliminating the need for external trim adjustment and providing significant advantages in terms of cost, reliability and flexibility over conventional trimming techniques.

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[2] Holt, J.G., "A Two-Quadrant Analog Multiplier Integrated Circuit", IEEE J. Solid-State Circuits, vol. SC-8, pp. 434-439, December 1973.

III. LOGARITHMIC AMPLIFIERS

A. GENERAL DESCRIPTION

Logarithmic amplifiers are useful in many areas of signal processing, when it is necessary to develop log functions of an input signal.

The most suitable non linear element used for log operation is the bipolar transistor, since the relationship between collector current and emitter-base voltage is precisely logarithmic from currents below 1 picoampere up to currents of the order of 1 milliampere. The presently available solid state logarithmic amplifiers use a matched pair of transistors plus operational amplifiers and resistors to implement their transfer functions, with a dynamic range in excess of five decades.

Typical logarithmic operations and idealized transfer functions are listed below:

$$e_o = -K \log \frac{e_{in}}{E_{REF}} \quad ; \text{ log of voltage}$$

$$e_o = -K \log \frac{i_{in}}{I_{REF}} \quad ; \text{ log of current}$$

$$e_o = E_{REF} 10^{\frac{-e_{in}}{K}} \quad ; \text{ antilog of voltage}$$

$$e_o = -K \log \frac{i_{in}}{i_{ref}} \quad ; \text{ current log ratio}$$

$$e_o = -K \log \frac{e_{in}}{e_{ref}} \quad ; \text{ voltage log ratio}$$

where K is the scale factor, e_{in} and e_{ref} are, respectively, the input and reference voltages (continuously variable), E_{REF} is the DC reference voltage, i_{in} and i_{ref} are, respectively, the input and reference currents (continuously variable), and I_{REF} is the DC reference current.

Specifications which must be considered when analyzing log amplifiers are defined as follows:

Log Conformity describes how well the logging elements conform to the ideal log transfer characteristic and is expressed as percentage of the input signal.

Dynamic Range is the range of input voltages or currents over which the device is guaranteed to operate.

Scale Factor is defined as the voltage change at the output for a decade change at the input of the amplifier.

Offset can be described as the output voltage in the absence of signals at the input terminals.

Temperature Stability is normally specified in terms of temperature drift of scale factor and offset voltage.

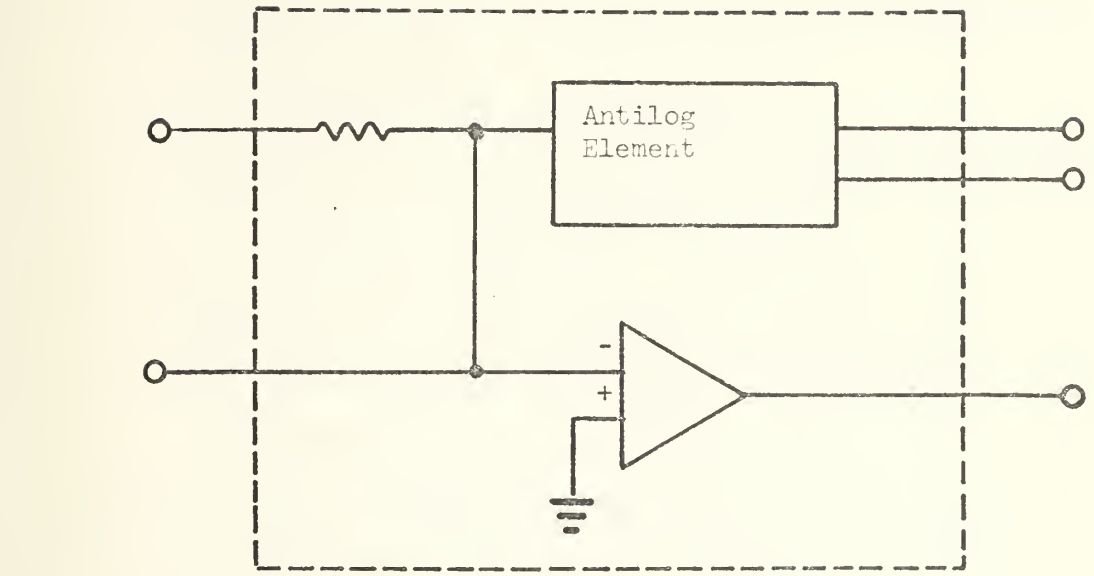
Small-Signal 3 db Bandwidth is the frequency at which the output is 3db down from its reference value, for a constant input level.

B. APPLICATIONS

Logarithmic amplifiers have a wide range of applications in signal processing. There are three major types of circuits which perform logarithmic operations:

1. Log and antilog amplifiers
2. Log ratio amplifiers
3. Special purpose circuits

Log and antilog amplifiers are the basic blocks for logarithmic operations. The combination of log amplifiers and operational amplifiers within a module is used to perform log ratio functions, as shown in Fig. 2.



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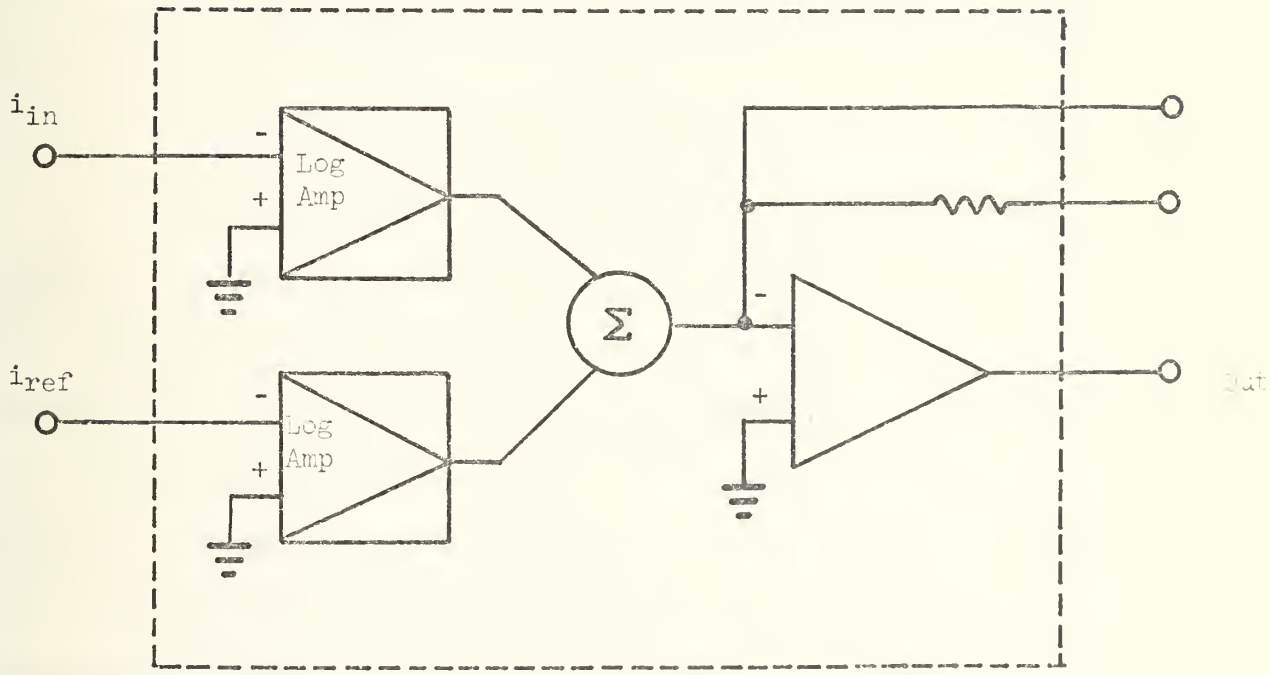


(b)

Figure 2. Functional block diagrams: (a) log and antilog amplifiers, (b) log ratio amplifier

Some of the uses for log, antilog and log ratio amplifiers are:

1. Signal Compression
2. Exponentiation and root extraction
3. Photometry: direct calculation of absorbance, linearization of exponential measurements, etc.
4. Normalization of signals having wide dynamic range
5. Displaying gain measurements in logarithmic form (e.g., "dB")

Special purpose logarithmic circuits perform different log operations for each particular application. These devices work on a log network principle, combining logarithmic circuits as building blocks to implement their transfer functions. Some of the most widely-used special purpose log circuits are:

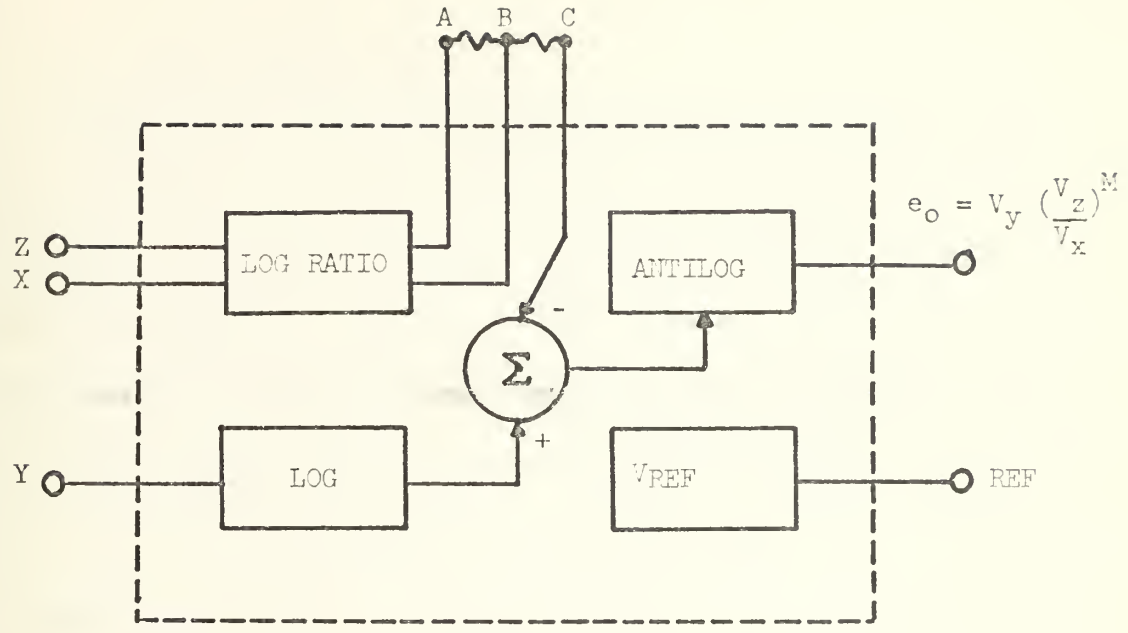
1. Programmable multifunction converters

Multifunction converters usually combine log, log ratio, and antilog circuits as shown in Figure 3 to achieve the transfer function $E_o = V_y(\frac{V_z}{V_x})^m$. These circuits are capable to produce the functions of multiplication, division, exponentiation, square-rooting, squaring, sine, cosine, arc-tangent, and vector algebra. They are generally designed to be used for transducer linearization in medical, industrial, and process control equipment. Other applications include analog processing of data as an input to data acquisition systems, data compression in analog systems, vector computation, and rectangular-to-polar coordinate conversion.

2. RMS-to-DC converters

The functional block of a typical RMS-to-DC converter is

converter is shown in Figure 3b). Some applications are complex waveform measurements, precision line regulation, random thermal noise and power supply ripple measurements.



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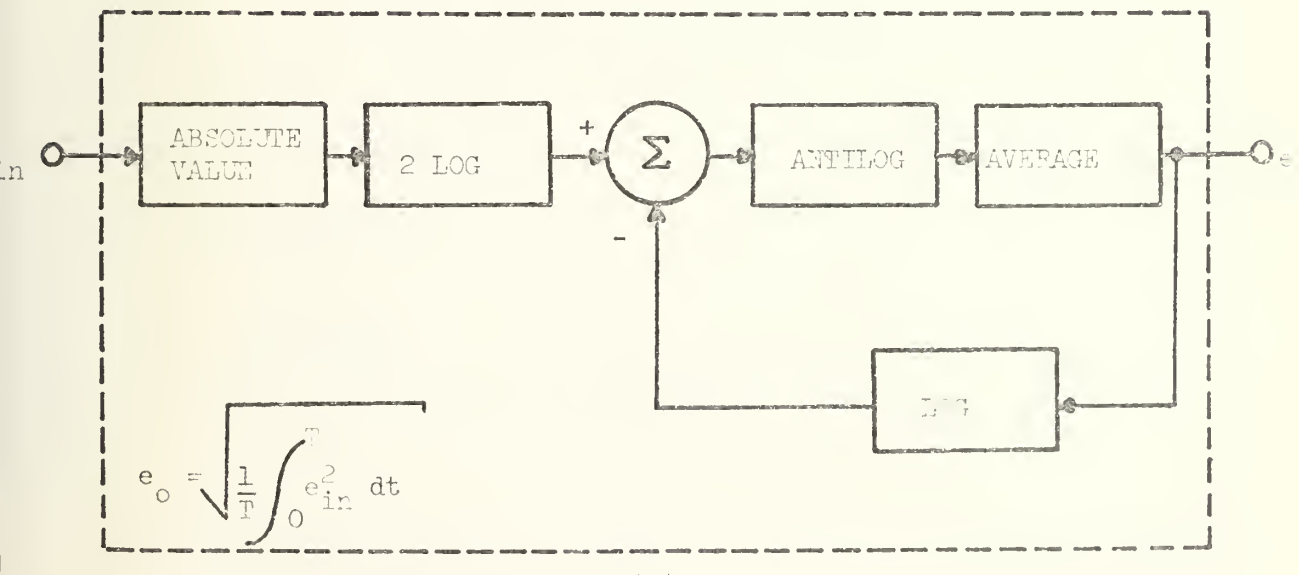

(b)

Figure 3. Functional Block Diagrams of Special Purpose Log Circuits

3. AC log amplifiers

These devices produce an output voltage proportional to the inverse hyperbolic sine of the input signal. The resulting function is logarithmic for larger values of input, but it passes through zero essentially linearly. They are used for compression of bipolar functions, and in applications where a very wide dynamic range signal must be recorded or transmitted, or a nonsaturating amplifier is needed such as in speech communications.

C. CIRCUIT TECHNIQUES

The logging technique most suitable for integration is the "matched transistors" method. It is derived from the inherent exponential characteristics of a transistor junction, and provides an accurate function over many decades. Temperature dependency can be reduced significantly by using carefully-selected monolithic pairs and temperature-sensitive gain elements. In fact, the high performance associated with this technique is obtained to the extent that logging transistors are matched to each other.

D. STATE-OF-THE-ART

1. Performance

Table IV lists typical specifications of basic log amplifiers.

Table IV

State-of-the-Art in logarithmic amplifiers (typical values)

Specification		Performance
Log Conformity		
	Current ($\pm$)	0.5% to 1%
	Voltage ($\pm$)	0.5% to 1%
Dynamic Range		
	Current	1 nA to 1 mA (120 db)
	Voltage	1 mV to 10 V (80 db)
Scale Factor Drift ($\pm$)		0.04 %/°C
Offset Drift ($\pm$)		100 to 300 uV/°C
Bandwidth (-3 db, small-signal)		
i_{in}		BW
1	nA	80 Hz
100	nA	70 kHz
100	uA	180 kHz
1	mA	200 kHz

2. Technology

Log and antilog amplifiers are available in modular and monolithic IC construction. Monolithic fabrication of log and antilog circuits is a recent technology development. Using FET-input structures and thin-film resistor networks, trimmed on the chip, these amplifiers reap the benefit of low cost, small size and reliability associated with IC construction, for performance comparable to that of the modules.

Modular technology is also used in log ratio amplifiers,

multifunction converters, and all other log circuits; hybrid IC fabrication is presently available on multifunction circuits only.

IV. ANALOG-TO-DIGITAL CONVERTERS

A. GENERAL DESCRIPTION

Analog-to-digital converters are encoders that convert analog current or voltage signals to digital codes compatible with digital systems such as computers, telemetry links, simulators, decimal readout devices, control networks, etc.

The converter is therefore a key part of many industrial, commercial and military systems because it is the interface between analog systems and digital systems.

The following parameters are usually considered in the analysis of A/D converters:

Resolution is the relative value of the Least Significant Bit (LSB), or 2^{-n}, for n-bit converters. It may be expressed as 1 part in 2^n, as a percentage, in parts-per-million, or simply by "n" bits.

Absolute Accuracy defines the ability of a converter to translate from analog to digital with the analog voltage values referenced to the NBS voltage standard. Among the error components that reduce absolute accuracy are Gain or Scale Factor error and Offset error.

Relative Accuracy relates the analog voltage values to the reference used for controlling the slope of the converter transfer function, and is a measure of input/output linearity.

Nonlinearity is the maximum deviation from a straight line drawn between the endpoints of the input/output transfer function.

Differential Nonlinearity describes the variation in the analog value of transitions between adjacent pairs of digital numbers, over

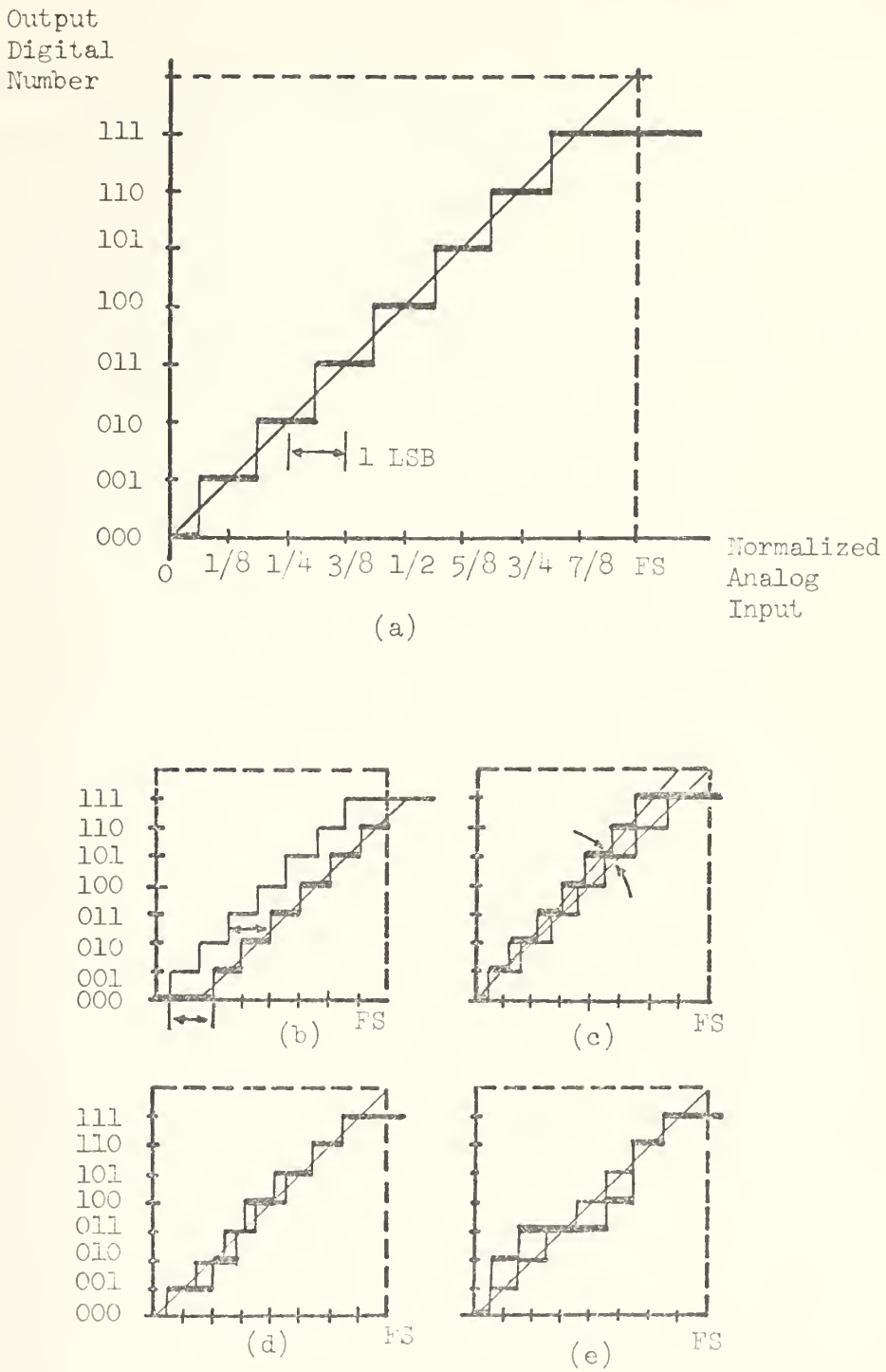

Figure 4. Conversion relationship in a 3-bit A/D converter: (a) ideal relationship, (b) offset error, (c) scale factor error, (d) linearity error, (e) missed codes

the full range of the digital output.

Gain or Scale Factor Stability is defined in terms of the deviation over a given temperature range. The total gain (or scale factor) change is normally specified in ppm/^{o}C.

Figure 4 shows the graph for an ideal 3-bit A/D converter, and typical sources of error.

B. APPLICATIONS

The use of integrated circuits has reduced the size, increased the capabilities, and also decreased the cost of A/D converters. These developments have subsequently expanded the practical uses of digital equipment in many areas, such as process control, aircraft control, telemetry, etc. Some of the applications of A/D converters are:

1. Data acquisition Systems
2. Digital voltmeters and digital weighting systems
3. Process or servo control systems
4. Time expansion
5. Transducers
6. Audio digitizing
7. Infinite track-hold amplifiers
8. Computer equipment
9. Medical electronic equipment
10. Radar and TV video digitizing

An analog-to-digital conversion applications guide is given in Table V.

TABLE V

A/D Converters Application Guide by Key Feature

Key Feature	A/D Converters Application
High speed, medium to high resolution	Data acquisition systems, test and measurement equipment, simultaneous sample-hold systems, conversion for data entry into digital filters and correlators.
High resolution and accuracy	Data acquisition systems with large number of low level data points.
High noise rejection, medium to high resolution and accuracy	Conversion of analog voltage levels such as transducer outputs of temperature, pressure, weight, position; data reduction for industrial and process control fields, oceanographical, geological and biomedical data.
Vary fast small-signal response	Time expansion, process or servo control systems, audio digitizers, track-hold amplifiers.
Low power, high reliability	Operation in remote areas with battery power (ocean buoy

	installation, seismology, remote meteorological data acquisition, pollution monitoring, etc); portable medical and scientific instrumentation.
Very high speed	Shipboard radar digitizing, digital removal of clutter from airborne radar, color TV video digitizing, auto correlation, pulse analysis, data logging, X-Ray analysis.
Economy, simplified operation, low speed	General purpose, OEM designs.

C. CIRCUIT TECHNIQUES

There is a large number of conceivable circuit designs for A/D converters. However, a much more limited number of designs is presently available in small, modular form, specifically suited for incorporation as components of equipment. The most common of these techniques are:

1. Successive approximation
2. Staircase or counter ramp
3. Dual slope integration
4. Tracking or servo
5. Parallel
6. Parallel/Serial

1. Successive Approximation

This conversion technique consists of comparing the analog input against a precisely-generated internal voltage at the output of a D/A converter; the input of the D/A converter is the digital number at the A/D converter's output. Successive approximation converters are quite widely used, especially for interfacing with computers, because they are capable of both high resolution and high speed.

2. Staircase or counter ramp

In this process, a reference voltage is integrated (while a counter counts clock pulses) until the output of the integrator is equal to the signal input. It is the simplest method currently in use, however, low cost and high reliability associated with it have to be weighted against the slow conversion and the fact that each

1-bit increase in resolution doubles the conversion time.

3. Dual Slope Integration

This method uses a indirect conversion technique, in which the input signal is converted to a proportional time interval, and then measured digitally. Dual slope integration has many advantages, such as excellent differential linearity, good noise rejection and low cost but the conversion time is generally high.

4. Tracking or Servo

Tracking or servo converters combine a D/A converter and a up-down counter. If the output of the D/A converter is less than the analog input, the counter counts up; if greater, the counter counts down. For a constant input, the counter output changes back and forth between the two adjacent bit values. This converter can follow small changes quite rapidly (it will follow 1 LSB changes at clock rate), but it will require the entire count to acquire full-scale step changes.

5. Parallel

The fastest A/D technique available is the parallel conversion. It uses a separate analog comparator with a fixed reference for every quantization level in the digital word, from zero to full-scale. Then, the outputs of these comparators are appropriately interconnected by the encoding logic circuitry to produce a parallel digital output. For n-bit resolution, 2^n -1 separate comparators and reference levels are needed. Thus, the system complexity increases very rapidly as the number of parallel bits is increased. In this type of converter, all input bits are processed simultaneously; therefore, the

entire encoding operation can be performed within one clock cycle. For resolution beyond 4 bits (i.e., 16 comparators and 16 separate voltage references), the parallel converters become impractical due to overall circuit complexity.

6. Parallel/Serial

To overcome the increased complexity associated with high resolution in parallel converters, a serial/parallel approach was developed. It uses a combination of parallel and successive approximation techniques, i.e., 2- or 3- bit parallel converter sections as building blocks in forming a successive approximation converter.

Table VI shows a comparison of A/D conversion techniques, listing their typical performances in four areas - resolution, accuracy, conversion time and stability.

Table VI

Comparative Characteristics of A/D Converters Types and Classes
(typical values)

Type	Performance Class	Resolution bits	Accuracy % of F.S.	Conversion Time usec	Gain Stability ppm/°C
Successive Approx.	General Purpose Low Cost	8 to 12	0.0125 to 0.5	15 to 100	15 to 50
	High Performance Moderate Cost	6 to 12	0.0125 to 0.8	4 to 30	5 to 40
	High Speed	8 to 12	0.0125 to 0.4	1 to 10	5 to 40
	Fast	4 to 12	0.025 to 3	0.4 to 2	20 to 50
	High Resolution	13 to 16	0.0015 to 0.005	8 to 400	6 to 15
	Low Power	8 to 12	0.01 to 0.4	60 to 130	20 to 50
Dual Slope Integrating	Medium Resolution	8 to 12	0.01 to 0.25	300 to 20,000	10 to 70
	High Resolution	14 to 17	0.0015 to 0.016	2,000 to 200,000	5 to 50
Staircase or Digital Ramp	General Purpose Low Cost	6 to 8	0.2 to 0.8	50 to 1,000	50 to 100
Parallel	Fast	4	6	0.02	300
Parallel/ Serial	Fast	4 to 10	0.1 to 3	0.06 to 0.2	50 to 100
Tracking	Medium Resolution	8 to 10	0.05 to 0.2	0.125 LSB	60 to 100

D. STATE-OF-THE-ART

1. Performance

Table VII describes the current state-of-the-art in resolution, speed and stability of A/D converters.

Table VII

State-of-the-art in A/D converters (best values)

Specification	Performance	Method
Resolution	16 Bits	Successive Approximation
	17 Bits	Dual Slope Integration
Conversion Time	20 nanosec	Parallel (4 bits)
	60 nanosec	Serial/parallel (10 bits)
Gain Drift	5 ppm/^{o}C	Dual Slope Integration, Successive Approximation, (Modular Fabrication)
	1 ppm/^{o}C	Successive Approximation (Hybrid Fabrication)

2. Technology

Hybrid technology, presently available in successive approximation A/D converters only, uses thin or thick-film processes to build the integrated arrays of precision resistors. Thick-film A/D converters utilize cermet passive elements composed of glass and precious metals fused to a 96% alumina substrate, featuring a temperature-coefficient tracking of 15 ppm/^{o}C and tolerance up to 0.2%. Thin-film devices use nickel-chromium or tantalum nitride resistor layers deposited on silicon. After the circuit has been assembled, the resistors

are laser-trimmed with an accuracy to within 0.01%. A temperature-coefficient tracking of 1 ppm/^{o}C is then achieved, resulting in converters with performance specifications that are stable over the entire operating temperature range. The factory trimming also eliminates the need for external adjustments.

Modular fabrication is used in all A/D conversion types, and only few models of hybrid IC successive approximation converters are currently available.

A recent development in A/D converters uses CMOS technology to produce low power successive approximation modules consumming 30 to 50 mW. In addition of low power requirements, the hybrid version of these CMOS converters has adjustment-free capability, which makes these devices highly suitable for many remote applications.

V. DIGITAL-TO-ANALOG CONVERTERS

A. GENERAL DESCRIPTION

Digital-to-analog converters are used to reconstitute the original data after processing, storage or even simple transmission from one location to another in digital form. A D/A converter can be considered as a decoding device which accepts a digitally coded signal D and an analog signal P as inputs and provides an analog output A related to the input as:

$$A = P.D \qquad (1)$$

The actual implementation of a D/A system contains four separate parts: a reference quantity (normally a voltage), corresponding to parameter P of Eq. (1); a set of binary switches to simulate binary coefficients; a resistive weighting network; and an output summing means.

The basic parameters used in describing D/A converters performance are defined below:

Resolution indicates the number of possible analog levels available. It is normally specified as the total number of input bits the converter will handle. For n-bit resolution, the converter must be capable of producing 2^n discrete analog output levels.

Absolute Accuracy is a measure of the deviation of the analog output level from its predicted value.

Relative Accuracy error is the difference between the nominal and actual ratios to full-scale of the analog value corresponding to a given digital input. This error is a function of the linearity of the

converter, and is usually specified at less than $\frac{1}{2}$ LSB.

Nonlinearity is the deviation from a straight line drawn through the end points of the transfer function.

Differential Nonlinearity describes the variation in the analog value of transitions between adjacent pairs of digital numbers, over the full range of the digital output.

Settling time is the time interval for a D/A converter to settle for a full-scale code change, usually to within $\pm \frac{1}{2}$ LSB. Settling time determines the overall response speed of the converter.

Monotonicity implies that the output of the converter, in response to a continuously increasing input signal, should not, at any point, decrease or skip one or more codes. Monotonic behaviour requires that the differential nonlinearity be 1 LSB.

Gain or Scale Factor Stability is defined in terms of the deviation over a specified temperature range, and is usually given in ppm/^{o}C.

Glitch or transient spikes occur in all D/A converters when it changes from one level to another. Deglitcher is a circuit that removes glitches. It normally consists of a sample-hold circuit which holds the output constant until the switches reach equilibrium.

A Multiplying D/A converter differs from the conventional fixed-reference converter in being designed to operate with varying (or AC) reference signals. The output signal of such a converter is proportional to the product of the reference voltage and the fractional equivalent of the digital input number. Four-quadrant multiplication is available if the D/A converter accepts reference signals of both positive and negative polarities, and the digital response is bi-

polar.

Figure 5 shows the graph for an ideal 3-bit D/A converter and typical sources of error.

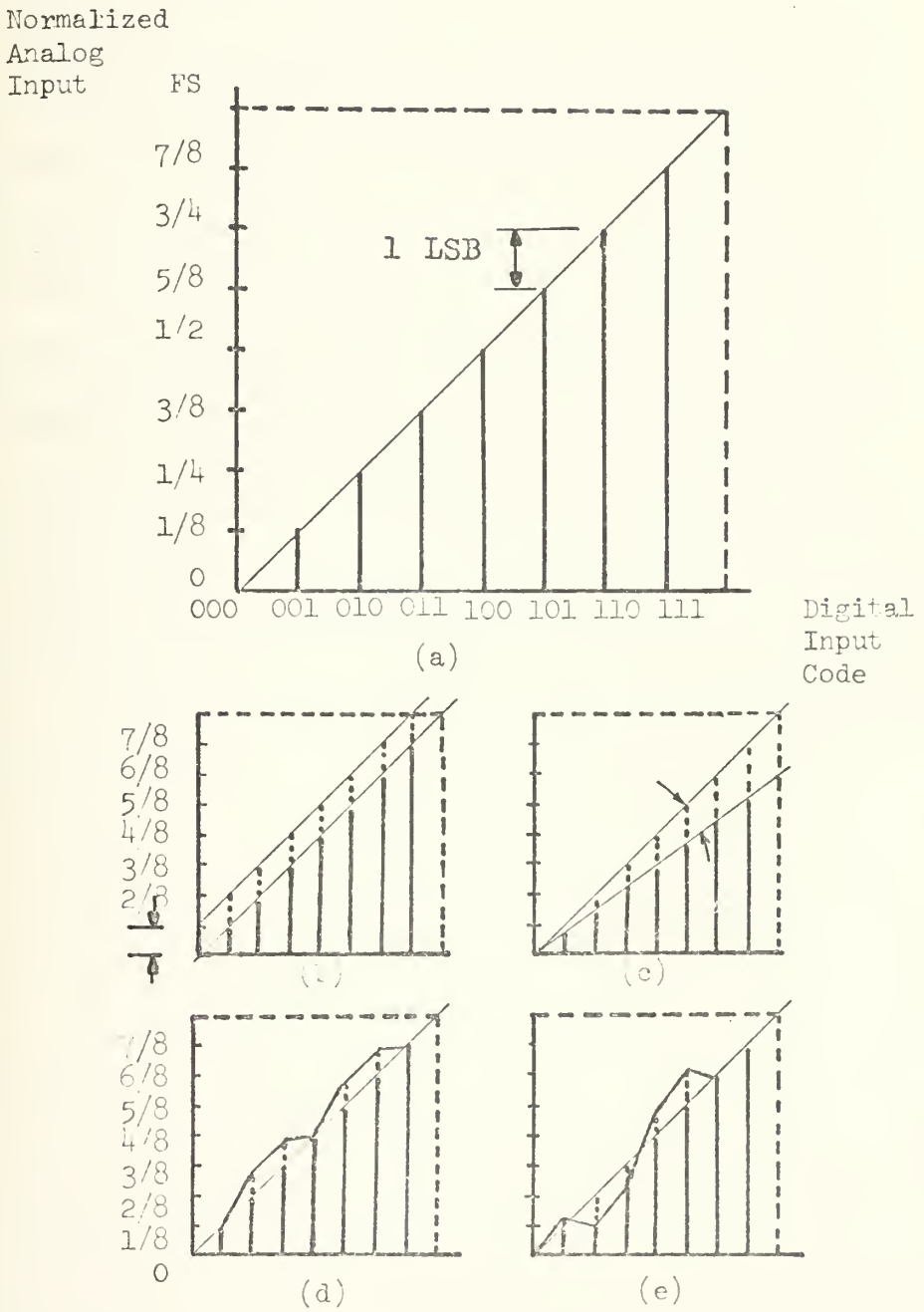

Figure 5. Conversion relationship in a 3-bit D/A converter: (a) ideal relationship, (b) offset error, (c) scale factor error, (d) linearity error, (e) non-monotonicity

B. APPLICATIONS

Digital/Analog converters are widely-employed in many fields using digital equipment. Some of their applications are:

1. Data distribution systems
2. Automatic test systems
3. CRT displays
4. A/D converters
5. X-Y plotters
6. Communications and signal analysis
7. Navigation systems
8. Computer equipment
9. Test equipment
10. Servo positioning systems

Table VIII lists a few applications of D/A converters by dominant parameter.

Table VIII

D/A Converters Application Guide by Key Feature

Key Feature	D/A Converters Application
High resolution and accuracy	High precision automatic test systems, precise analog function generation, systems and equipment demanding wide dynamic range.
Multiplying operation	Character generation for CRT, hybrid computation, radar display control, closed-loop control, digital phase shift and data normalization.
Fast settling speeds, glitchless	CRT displays, high-speed test equipments, A/D converters, X-Y plotters, function generators and programmers.
Low power	Portable medical and scientific instruments.
Moderate accuracy and settling time	Data transmission, semiconductor test equipment, programmed/ feedback control systems.

C. CIRCUIT TECHNIQUES

A basic D/A converter consists of a reference, a resistor network, a set of switches, and a summing operational amplifier, as shown in Figure 6. Several techniques are presently utilized to implement and combine these elements, depending on the requirements for each particular application.

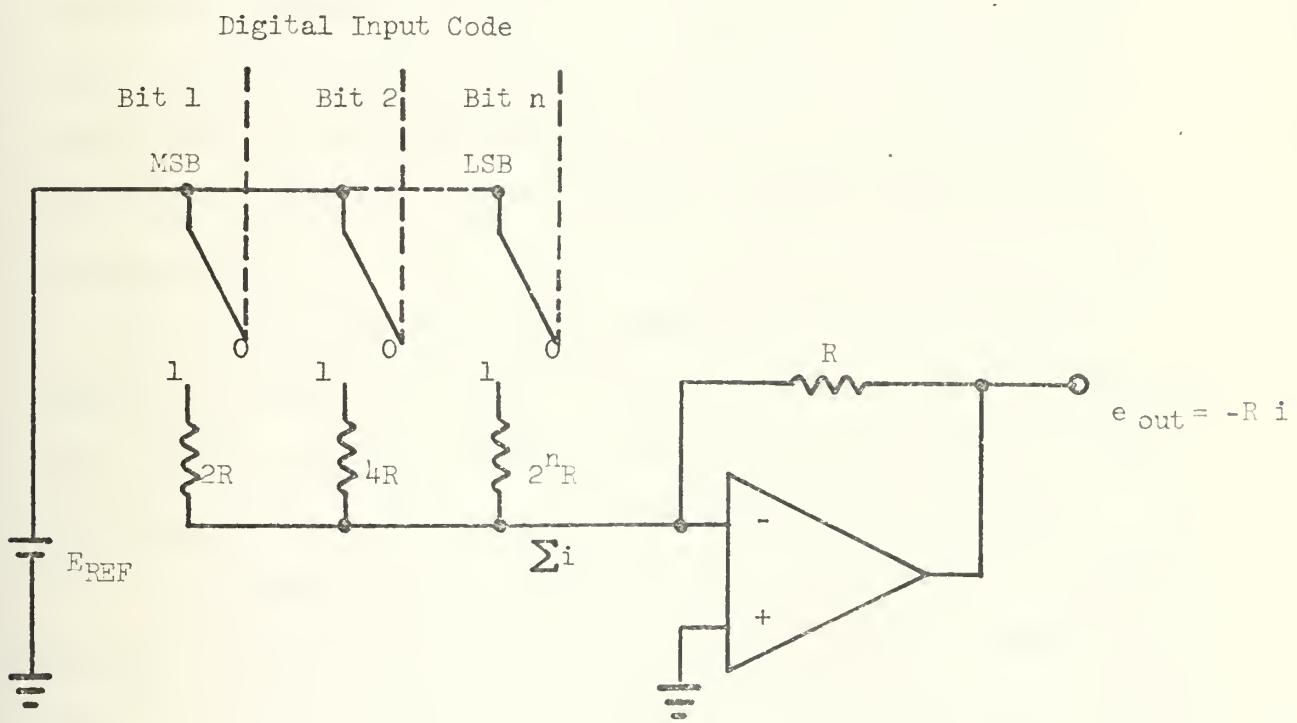

Figure 6. Elementary D/A converter circuit

Two major D/A conversion schemes are commonly used, the binary-weighted resistance network and the R-2R ladder network. Both methods use either current switching or voltage switching. Within each of these there are two sub-types: voltage output and current output. From the point of view of integrated circuits, some of these techniques

are usually combined as follows:

1. Binary-weighted network/Voltage switching
2. R-2R ladder/Voltage switching
3. R-2R ladder/Current switching (Equal current sources)
4. Binary-weighted network/Current switching (Weighted current sources)

Current switching is normally preferred over voltage switching in most applications, particularly in integrated circuits, because it offers significant speed advantages. A number of current-switching designs have been developed which are readily suited for monolithic integration, using either equal current or binary-weighted current sources schemes.

Voltage switching designs are simpler and lower in cost than current switching. They also are suited for applications where signals vary. Since they accept reference voltage of either polarity, they can be used, for example, in 4-quad multiplying D/A converters.

A converter can be built to produce either current or voltage output. The basic conversion process develops a current output that is very fast and better suited for some high speed applications such as CRT deflection amplifiers. Voltage output can be obtained from a built-in or external amplifier with inherently slower response added by the operational amplifier.

1. Binary-Weighted Network/Voltage Switching

In this configuration, the current weighting function is achieved by using n parallel, independent branches in the weighting network which have respective impedance levels of R, 2R, 4R, 8R etc.

Therefore, the spread of resistor values increases very rapidly as the resolution increases. In integrated thin or thick-film circuits, this technique is impractical for resolution higher than 6 bits. However, the weighted-resistors networks are better suited for design of 4-bit converter sections which can then be cascaded as building blocks to form higher-order converters.

2. R-2R Ladder/Voltage Switching

An alternate resistor configuration which eliminates the large component spread of the binary-weighted resistor networks is the ladder R-2R network. Since only two values of resistance are used in the ladder network, constant resistance ratios, and therefore, accurate output voltages can be maintained over large operational ranges of temperature, and it is easily implemented in integrated circuit form.

3. R-R2 Ladder/Current Switching

A particular advantage of the R-2R ladder network is that it can be used in conjunction with equal value current sources to perform the A/D conversion. In monolithic circuits where excellent matching can be obtained between devices of the same geometry and operating at the same level, equal current D/A conversion offers significant advantages, particularly for circuits having resolution of 8 bits or more.

4. Binary-Weighted Network/Current Switching

Commonly known as the quad current-source or weighted-current sources approach, this technique relies on binary-weighted current sources, cascaded in groups of four. The switches and resistors

are grouped in quads with repeated 2R, 4R, 8R, 16R resistance values and 8:1 maximum range of bit currents. An important benefit of the quad structure is that there are only 4 different current values, reducing the dimensions of the current matching problem, and maintaining adequate switching speed.

D. STATE-OF-THE-ART

1. Performance

A large number of integrated D/A converters is currently available from several manufacturers. Most of these designs are presently built in a modular form. However, in the low and medium resolution, hybrid (6 to 13 bits) and monolithic (6 to 10 bits) converters are gaining wide acceptance. A comparison of these fabrication techniques is given in Table IX, listing their typical performances in four areas - resolution, accuracy, settling time and stability.

Table IX

Comparative Characteristics of D/A Converters Types and Classes
(typical values)

Performance Class	Type	Resolution bits	Accuracy % of F.S.	Settling Time usec	Gain Stability ppm/^{o}C
General Purpose Low Cost	Modular	8 to 12	0.01 to 0.02	0.3 to 50	12 to 100
	Hybrid	6 to 12	0.01 to 0.8	1 to 50	1 to 50
	Monolithic	6 to 10	0.05 to 0.8	1.5 to 3	15 to 120
High Performance Moderate Cost	Modular	8 to 12	0.01 to 0.2	0.15 to 5	7 to 40
	Hybrid	-	-	-	-
	Monolithic	-	-	-	-
Fast	Modular	8 to 13	0.01 to 0.2	0.025 to 0.5	10 to 50
	Hybrid	8 to 13	0.01 to 0.2	0.1 to 0.5	1
	Monolithic	-	-	-	-
High Resolution	Modular	14 to 16	0.0015 to 0.01	1 to 250	1.5 to 30
	Hybrid	-	-	-	-
	Monolithic	-	-	-	-
Multiplying	Modular	8 to 12	0.01 to 0.2	0.05 to 15	11 to 30
	Hybrid	8 to 13	0.01 to 0.4	10 to 45	1 to 15
	Monolithic	-	-	-	-
Deglitched	Modular	12 to 14	0.003 to 0.01	5 to 20	7 to 20
	Hybrid	13	0.05 to 0.01	50 ns for 1 LSB	10
	Monolithic	-	-	-	-

2. Technology

Hybrid technology uses thin or thick-film processes in the precision resistance networks fabrication. Thin-film materials currently employed are nichrome, tantalum, and various cermets; the most commonly used substrates are silicon, alumina and glass. Laser-trimming to 0.01% is normally performed, allowing a typical temperature-coefficient tracking of 1-2 ppm/^{o}C and adjustment-free operation of the associated converters. Most thick-film hybrid D/A converters use cermet material fused to alumina substrate; typical temperature coefficient is 10-20 ppm/^{o}C.

Today's monolithic D/A converters generally include voltage reference, resistance network and current source/switches, in one or two monolithic chips. In some designs, the summing amplifier is left external to the chip. CMOS technology is a recent development in monolithic D/A conversion; it can provide 10-bit resolution, 5 to 10 ppm/^{o}C temperature-coefficient and low power consumption at low cost. A typical CMOS Multiplying converter uses R-2R thin-film ladder composed of silicon-chromium resistors deposited on the CMOS die. It consists of 10 CMOS switches and a thin-film-on-CMOS ladder network, featuring settling time of 500 ns and 5 ppm/^{o}C temperature-coefficient.

VI. SAMPLE-HOLD AMPLIFIERS

A. GENERAL DESCRIPTION

To sample and hold typically means to sample the value of a changing signal at a particular point in time and store this value until the next sample is taken. A Sample-Hold module is a device having a signal input, an output, and a control input, with two steady-state operating modes. In the Sample mode, it acquires the input signal as rapidly as possible an tracks it precisely until commanded to Hold. At this time, in the Hold mode, it retains the value of the input signal present when the control signal called for a mode change, as shown in Figure 7. Sample-Hold devices are known as "Track-Holds" if they spend the major portion of the time in sample mode, tracking the input. The control inputs are operated by logic levels; logic "1" is usually the sample command and logic "0" the hold command.

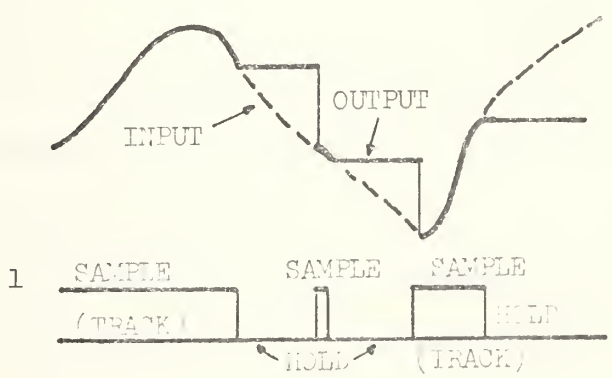

Figure 7. Typical sample-hold waveforms

Typical parameters of Sample-Hold devices are usually defined in four states: Sample, Hold, and the Sample-to-Hold/Hold-to-Sample transitions.

During Sample state:

Nonlinearity is the amount by which the input/output transfer function deviates from a "best straight line".

Settling time can be described as the time required for the output to attain its final value within a specified value of full-scale when a full-scale input step is applied.

During Sample-to-Hold transition:

Aperture time is the apparent time elapsed between the Hold command and the effective opening of the Hold switch. It has two components, a nominal delay and a uncertainty caused by jitter or variation from time-to-time or unit-to-unit.

Settling time is defined as the interval required for the output to attain its final value within a specified fraction of full-scale, following the opening of the switch.

During Hold state:

Droop or decay rate is the drift of the output at an approximately constant rate caused by the flow of current through the storage capacitor.

During Hold-to-Sample transition:

Acquisition time is defined as the length of time between the Sample command and the moment the output is tracked within the specified accuracy.

B. APPLICATIONS

Sample-Holds are most-widely used in data acquisition systems,

either to "freeze" fast moving signals during conversion or to store multiplexer outputs while the signal is being converted and the multiplexer is seeking the next signal to be converted. In analog data-reduction, they are used to determine peaks or valleys, establish amplitudes in resolver-to-digital conversion, and facilitate analog computations involving signals obtained at different instants of time. In data-distribution systems, Sample-Holds can be employed for holding converted data between updates of to diglitch D/A converters in systems that are sensitive to spikes.

C. CIRCUIT TECHNIQES

The choice of storage element divides Sample-Hold devices into two major classes: Analog and Digital. Analog techniques employ a capacitor for storage, are lower in cost and widely used. Digital storage uses an A/D converter and a register for storage, and reads out via a D/A converter; is more complex and costly, and its significant advantage is an arbitrary and essentially "infinite" hold time. The most common analog storage designs use the Open-loop follower or Feedback techniques.

1. Open-Loop Follower

This amplifier consists of an input buffer, a switch, a capacitor and an operational amplifier, as shown in Figure 8a). When the switch is closed, the capacitor charges exponentially to the input voltage, and the amplifier's output follows the voltage of the capacitor. When the switch is opened, the charge remains in the capacitor. An input Buffer (follower) is used to avoid input source loading by the capacitor. This technique produces fast acquisition

and settling but low-frequency tracking accuracy is moderate.

2. Feedback Circuits

High accuracy in low-frequency tracking can be accomplished by closing the loop around a storage capacitor, and using high loop gain to enforce tracking accuracy. Figure 8b) shows a configuration in which the input follower is replaced by a high gain difference amplifier. In Figure 8c), an integrator is used, permitting the switch to operate at ground potential, simplifying leakage problems. In feedback techniques, the charge on the capacitor is controlled by the output, as well as the input, and the acquisition time is equal to the settling time.

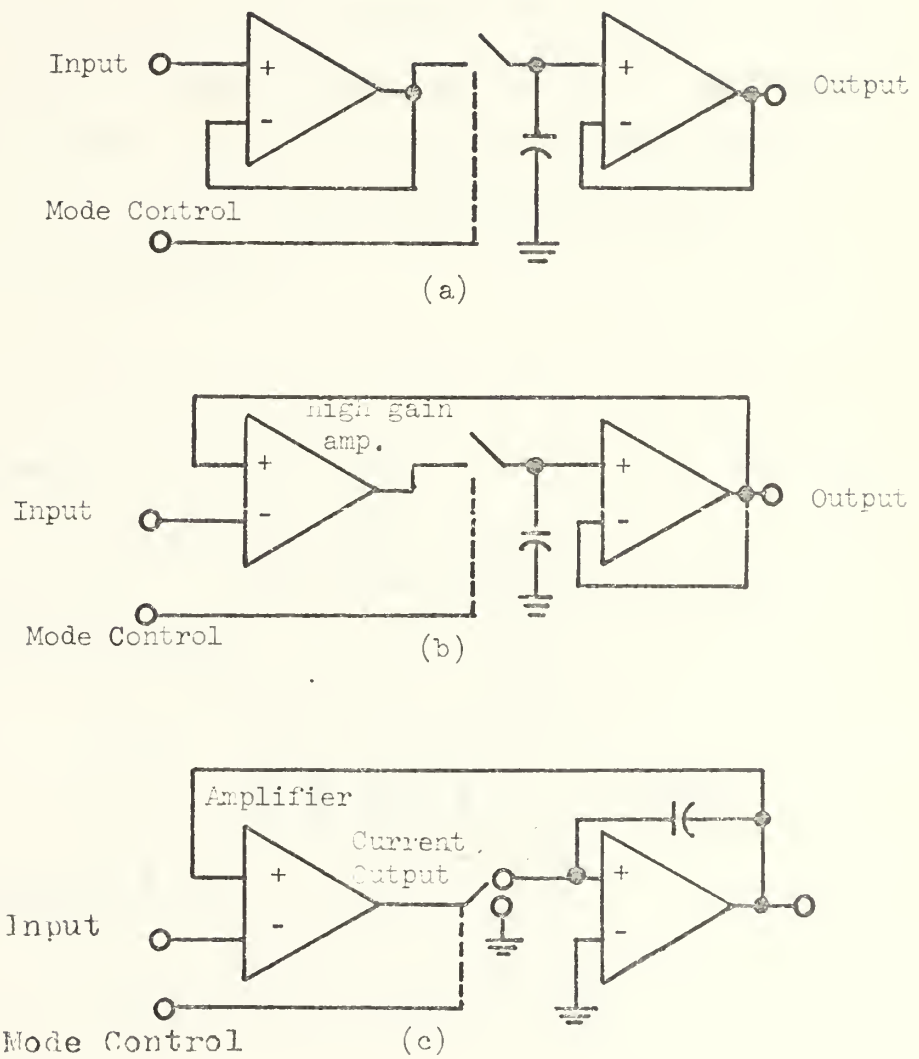

Figure 8. Analog storage sample-hold configuration: (a) open-loop follower, (b) feedback (non-inverting), (c) feedback (inverting)

3. Digital Storage

This technique provides an arbitrarily-long hold duration with no droop, sample or hold offset, feedthrough, dielectric absorption effects, or sample-to-hold transients, since the system is automatically in hold after a conversion, unless a Sample command is applied. In addition,both analog and digital outputs are available. Disadvantages are increased cost, higher complexity, and typically longer acquisition time. Figure 9 shows a digital storage Sample-Hold amplifier, using an A/D and a D/A converters.

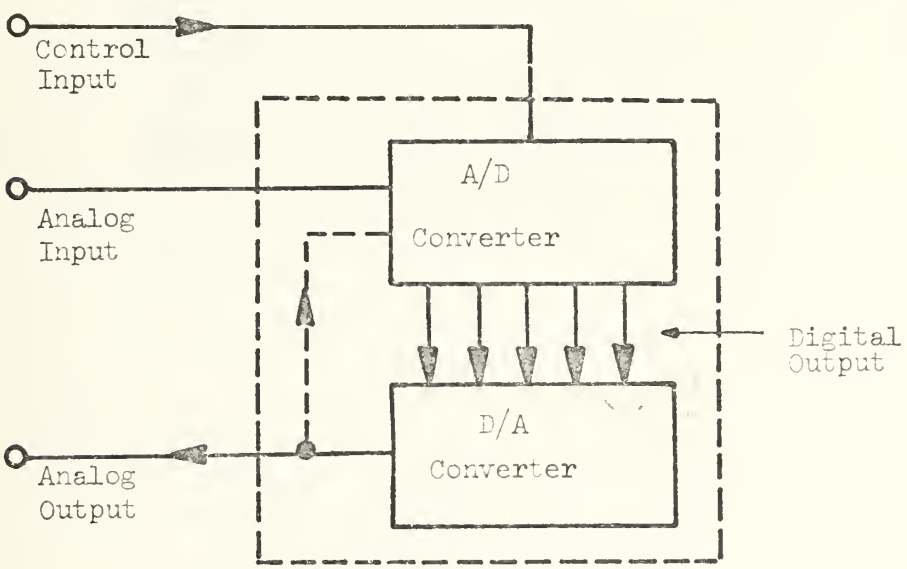

Figure 9. Sample-hold using A/D and D/A converters

Table X lists typical specifications of Sample-Hold amplifiers using analog and digital storage techniques.

Table X

Comparative Characteristics of Sample-Hold Amplifiers Types and Classes
(Typical values)

Performance Class	Type	Acqusition Time to $\pm\frac{1}{2}$ LSB usec	Droop Rate mV/sec	Aperture Time nsec	Linearity % of F.S.
Low Droop	Feedback	15 to 130	5 to 10	40 to 50	0.01
	Open-Loop Follower	10 to 100	0.25 to 15	20 to 150	0.01 to 0.015
General Purpose Low Cost	Feedback	70	10^3	20	0.01
	Open-Loop Follower	35 to 50	20 to 10^3	50 to 100	0.01 to 0.015
Medium Speed	Feedback	4 to 10	10 to $5X10^3$	45 to 100	0.01 to 0.015
	Open-Loop Follower	4 to 20	20 to 10^3	40 to 100	0.005 to 0.02
Fast Acquisition	Feedback	0.5 to 1	100 to $2X10^3$	5 to 10	0.005 to 0.01
	Open-Loop Follower	0.015 to 0.15	10^3 to $50X10^3$	0.1 to 10	0.1 to 0.5
Infinite Memory	Digital	1	0	1	0.8

D. STATE-OF-THE-ART

1. Performance

Table XI describes the current state-of-the-art in four significant specifications of Sample-Hold amplifiers: acquisition time, droop rate, aperture time, and linearity.

Table XI

State-of-the-Art in Sample-Hold Amplifiers (best values)

Specification	Performance	Method
Acquisition Time	15 nsec	Open-Loop Follower
Droop rate	0.25 mV/sec 0	Open-Loop Follower Digital
Aperture Time	100 picosec	Open-Loop Follower
Linearity	0.005%	Open-Loop Follower Feedback

2. Technology

Modular fabrication is used in all Sample-Hold types, and only few models of hybrid and monolithic amplifiers are currently available. Both hybrid and monolithic commercial Sample-Holds require the connection of an external holding capacitor to perform the storage function. Open-loop follower technique is employed in the only monolithic Sample-Hold available on market. It utilizes a MOSFET unity-gain amplifier as input buffer, featuring medium speed, low droop and reasonable performance at very low cost. A completely monolithic Sample-Hold (including storage capacitor) was recently reported,

which utilizes simultaneously fabricated bipolar transistors, low threshold P-channel silicon-gate field-effect transistors (SIGFETs), and SiO_2 dielectric capacitors on the same die.

Programmable gain Sample-Holds are available in modular form; they are used in data acquisition systems when incoming signal levels are too small to drive most A/D converters directly, eliminating the need for supplementary amplifiers.

VII. CHARGE-TRANSFER DEVICES

A. GENERAL DESCRIPTION

Storing and delaying analog signals have always presented a technological problem, particularly when a variable delay is required. Recently, charge-transfer devices (CTD's) have become available, which can be used as analog shift registers and give delays in the range 10^{-1} to 10^{-6} s. CTD's are analog, sampled data delay lines, and as such they are readily applicable to a large number of analog signal processing functions. Certain types of sampled data filters which have, up until now, been implemented digitally, can be realized in integrated form with CTD's.

CTD's include two important classes of device which are functionally very similar: Charge-coupled devices (CTD's) and bucket-brigade devices (BBD's). In CCD's, the charge to be transferred is stored in potential wells at the interface between silicon and silicon dioxide; in BBD's charge is stored in capacitors and is transferred from capacitor to capacitor through transistor action. BBD's can be fabricated using conventional MOS processes; CCD's require non-standard processing but they have performance advantages over BBD's and will probably dominate analog signal processing in the future.

The way in which a CCD can be operated as an analog shift register is illustrated in Figure 10. This figure shows schematically a device consisting of MOS electrodes that can be pulsed in sequence so as to move potential wells for minority carriers along the surface of the silicon. In the case shown, these wells contain packets of electrons;

once a charge packet of a particular size has been feed into one of the potential wells, it will be transferred, essentially intact, from under one electrode to the next and moved across the device.

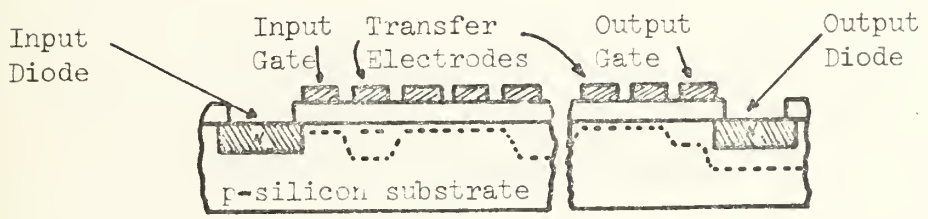

Figure 10. Schematic cross section of a CCD

Figure 11 shows how the electrodes of a IGFET BBD are driven, in a two-phase manner, in order to accomplish charge transfer. Each electrode, when pulsed on, capacitively reverse biases the diffusion immediately under it and inverts the channel between this diffusion and the neighbor. If one phase is turned on and the other is turned off, half of the diffusion acts as effective sources and the other half as drains, so that the excess charge transfer from one to another. At the next half cycle, each source becomes a drain and vice-versa, and the excess charges are once more passed along the line.

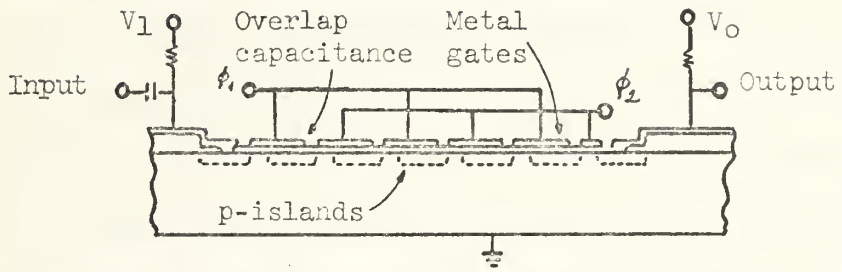

Figure 11. Representation of an IGFET bucket-brigade device

The most important parameters in the analisys of CTD's can be described as follows:

Transfer inefficiency is the fraction of a charge packet of a given size that is left behind per transfer. The effect of transfer inefficiency is to reduce the frequency response from its theoretical value and introduce dispersion in the signal. For a surface channel CCD, there are three types of loss which degrade the charge transfer efficiency: fixed loss, which usually results from a surface state trapping, is independent of signal amplitude, and can be eliminated

by a proper background charge or "fat zero"; proportional loss, which has many possible causes such as edge effect or transit time losses, is proportional to signal amplitude, and cannot be eliminated; non-linear loss, a general description of transfer loss including the dependence on signal amplitude, which can be nonlinear, and the loss caused by potential barriers in the interlectrode gap region.

Dark current is the attempt of the device to achieve an equil-ibrium condition by generating minority carriers to fill the potential wells. Since a filled well represents thermal equilibrium, if the well is not completely filled a dark current results which eventually fills the well. Properties of silicon, together with advanced state of silicon device processing technology permit the realization of dark current levels low enough for many CCD applications.

Noise sources in CCD's are grouped into four general categories: input noise, which is applied to the input and is attenuated by transfers through the entire device; leakage current noise, i.e., a noise that is continuously being added to a charge packet as it travels down the device; fast-interface-state noise, which results from a variance in the amount of charge transferred each clock period; and output noise, i.e., introduced after all transfers.

The maximum delay produced by a CTD is the number of elements N multiplied by the time $1/f_o$ for a charge packet to move one element, i.e., N/f_o, for a sampling frequency f_o. Hence, the maximum delay-bandwidth product for a CTD is $N/2$.

B. APPLICATIONS

Charge transfer devices are uniquely suited to many analog signal processing functions because they are capable of operating directly with analog signals. The largest impact which CTD's will make on signal processing is cost reduction of systems which are produced in sufficiently high volume to offset the development cost of custom CTD's. Charge transfer devices have also potential advantages in small size and low weight which result from their compactness, and in increased reliability resulting from a reduction in the number of package interconnections required. Analog applications of CTD's include imaging and signal processing, and the most important uses of CTD's in analog signal processing are as delay lines, transversal filters, and analog multiplexers, as described below.

1. Delay Lines

Significant advantages of CTD's as analog delay lines are that, in contrast to alternative approaches, the interface is compatible with integrated circuits and the amount of delay may be varied by changing the clock frequency. Some of the uses of CTD's delay lines are:

a. Video delay line for color TV.

b. Audio techniques used in artificial reverberation, public address systems, and speech systems.

c. Time-axis correction in recording systems.

d. Scanning of sensors or actuators arrays.

2. Transversal Filtering

A block diagram of a sampled data, transversal filter is shown in Figure 12. It consists of a sampling stage S followed by M-delay stages D, each of which delays the signal by a time equal to an integral number of clock periods T_c. The signal is nondestructively sampled at each delay stage, multiplied by the appropriate weighting coefficient h_k (k = 1,M), and the weighted signals are summed together to give the filter output. When an arbitrary signal $v_{in}(t)$ is applied to the filter, it can be shown that the filter output is

$$v_{out}(nT_c) \approx \int_o^{Td} h(\tau)\ v_{in}(nT_c - \tau)\, d\tau ,$$

where $v_{in}(kT_c)$ represents the sampled input signal, and T_d $(=MT_c)$ is the total time delay of the filter. This output is approximately equal to the convolution of the input signal with the impulse response of the filter.

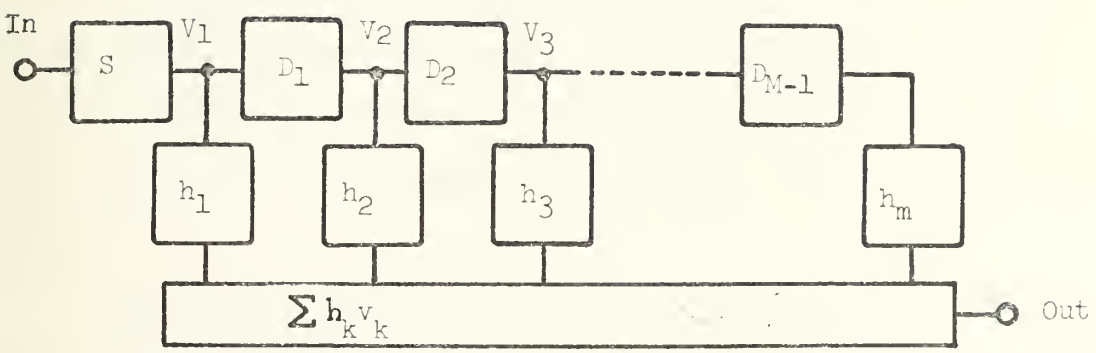

Figure 12. Transversal filter block diagram

Operationally, CTD transversal filters can perform the same functions as surface wave devices (SWD) transversal filters, except that SWD filters are limited in the time duration of the impulse response to a few tens of microseconds whereas CTD filters can process signals having hundreds of milliseconds time duration. CTD filters, on other hand, are limited in bandwidth to a few tens of megahertz (SWD's are used from 20 MHz to 1 GHz).

In order to implement a CTD transversal filter, it is necessary to nondestructively sample the delay line and to perform the weighted summation indicated in Figure 12. This is achieved in different ways, depending on whether CCD's or BBD's are used. Two techniques for performing sampling, weighting, and summing are currently used:[4] electrode weighting, for use primarily with CCD's, and gate tapping, used with BBD's. Filter programmability is very important for many systems applications, and the gate tapping method has the advantage of ease implementation of programmable (variable weighting) transversal filters.

Three major classes of CTD transversal filters are presently available: non-programmable (fixed weighting), digitally programmable, and analog programmable.

Non-programmable filters can be employed in matched filtering, bandpass filtering, Hilbert transform, complex coding, and real time Discrete Fourier Transform, as follows:

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[4] Buss, D.D., and others, "Transversal Filtering Using Charge-Transfer Devices", IEEE J. Solid-State Circuits, vol. SC-8, pp. 138-151, April 1973.

a. Matched Filtering

Matched filtering is widely-used in low data rate, spread spectrum communication systems where it is desired to transmit a peak-power-limited signal over a noisy channel. The peak power limitation is overcome by spreading the energy in a low-power signal over a long time interval (up to several hundred milliseconds in some applications). The receiver in such a system must be capable of coherently integrate the received signal power for the time duration of the signal, and it requires a matched filter. As indicated previously, CTD's are limited in frequency to tens of megahertz, therefore, filtering in a CTD system must be performed at baseband in distinction to SWD systems, where the filtering is performed at RF. A baseband system which can be used to detect binary chirp (linear FM) is shown in Figure 13, implemented with 200-stage BBD filters.[5] Chirp signaling system is used because it is minimally sensitive to error in the local oscillator frequency, and this is expected to be a major problem in CTD sproad spectrum systems. The filters marked SIN and COS in Figure 13 are matched to the chirp signals.

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[5] Buss, D.D. and Bailey, W.H., "Applications of Charge Transfer Devices to Communication", NELC CCD Applications Conference Proceedings, pp. 83-93, September 1973.

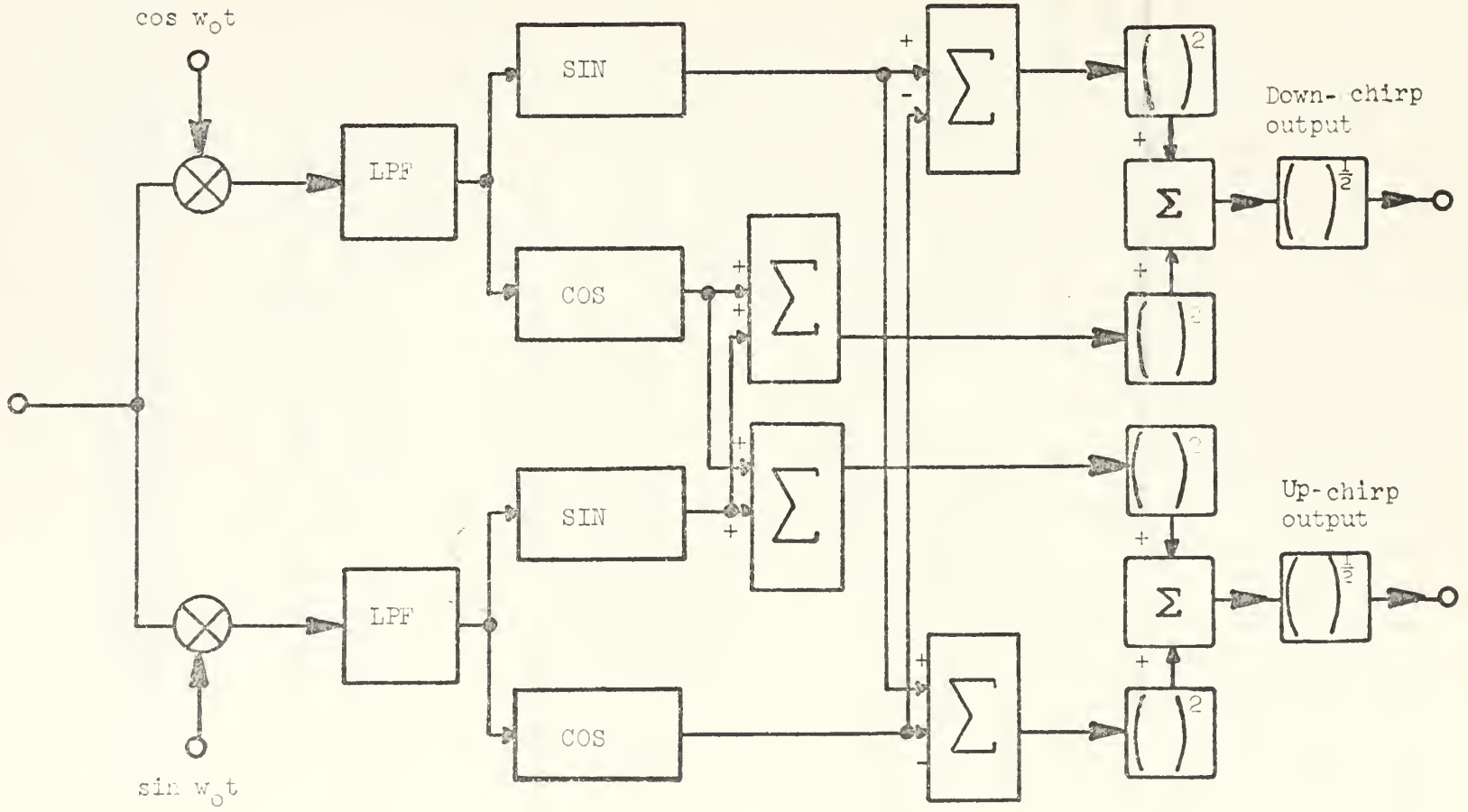

Figure 13. A receiver for binary chirp waveforms

b. Bandpass Filtering

Bandpass filters can be implemented with CTD transversal filters by selecting the impulse response of the filter to be the inverse transform of the frequency characteristic. A Dolph-Chebyshev filter was implemented with 101-stage CCD.[6] This class of filter is designed to optimize the trade-off between the width of the passband and the rejection outside the passband. It achieves 29 dB out-of-band rejection and a 3 dB bandwidth of 4% of the center frequency. The center frequency is designed to be $\frac{1}{4}$ of the clock frequency f_c and can be varied by varying f_c. The principal advantages of CTD transversal filters in spectral filtering are tunability and flexibility in selecting the spectral characteristic.

c. Hilbert Transform

A Hilbert Transform consists of a convolution with t^{-1} and can be implemented with a CTD transversal filter having the appropriated weighting coefficients. Such a filter can be used to generate single-sideband signals and has a wide potential application in communications.

d. Complex Coding

In complex coding, CTD filters are useful because they are capable to generate as well to detect arbitrary waveforms. This

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[6] Buss, D.D. and Bailey, W.H., "Applications of Charge Transfer Devices to Communication" NELC CCD Application Conference Proceedings, pp. 83-93, September 1973.

presents the possibility of choosing M waveforms to represent k = $\log_2 M$ bits of information. This type of coding is currently employed in MODEM's, but the choice of waveform is limited by the available equipment, and the waveforms actually used are not orthogonal or optimized to the transmission medium. CTD's offer a great deal of flexibility in selection of waveform. In addition, the relative ease with which CTD filters can be matched to arbitrary waveforms may make feasible the use of M-ary (instead of binary) communication where it has not previously been practical.

e. Real Time Discrete Fourier Transform

The technique of using CTD's to perform the Discrete Fourier Transform (DFT) of an electrical signal is the chirp-Z transform (CZT) method and involves multiplication and convolution with chirp signals. The CZT was first conceived as an algorithm for the DFT on a digital computer. It never gained acceptance, however, because the number of digital operations required for its implementation is the same as for the Cooley-Tukey Fast Fourier Transform (FFT) algorithm. A real time DFT device using BBD's was demonstrated[7] which is a factor of $\log_2 N$ faster than the FFT, N being the number of samples in the time signal. Figure 14 shows the system used to implement the CZT. Both SIN and COS filters are 200-stage BBD transversal filters used to perform the required convolution.

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7 Means, R.W., Buss, D.D., and Whitehouse, H.J., "Real Time Discrete Fourier Transforms Using Charge Transfer Devices", NELC CCD Applications Conference Proceedings, pp. 95-101, September 1973.

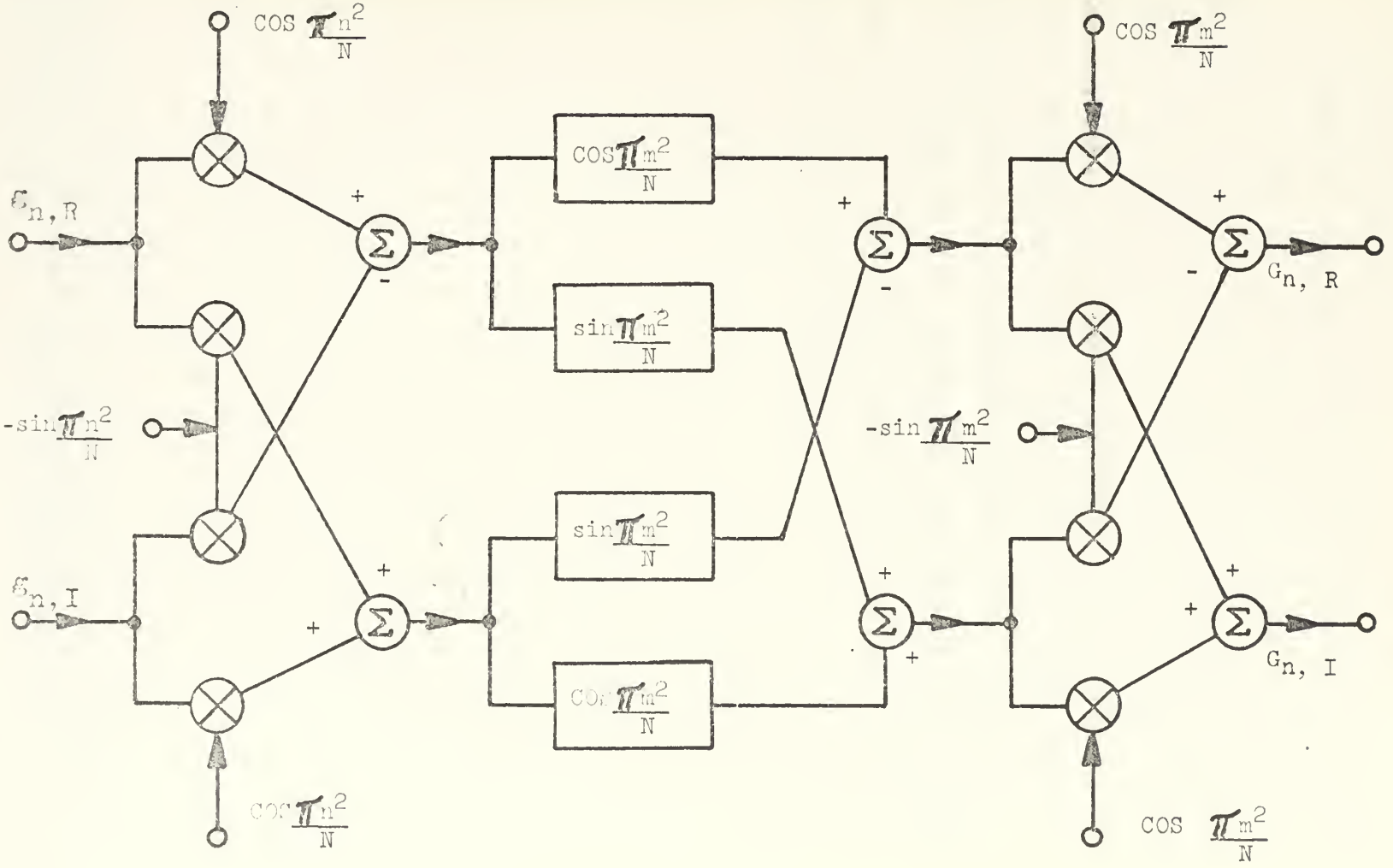

Figure 14. Discrete Fourier Transform via CZT algorithm

f. Cross Correlation

Digitally Programmable transversal filters are primarily used in cross-correlation applications such as spread spectrum communication and secure systems.[8] This multilevel detector takes an input analog signal and separates it into in-phase (I) and quadrature phase (Q) components; both I and Q channels are then digitized and each level of each channel is then separately correlated with the corresponding level of the digitized reference code. Figure 15 shows the implementation of a correlation detector suited to a radar pulse coded with a 512-bit pseudo-random sequence which is used to biphase-modulate a 60 MHz IF carrier.

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[8] Zimmerman, T.A., and Bower, R.A., "The Use of CCD Correlators is a Spread Spectrum Communications Example", NELC CCD Applications Conference Proceedings, pp. 141-146, September 1973.

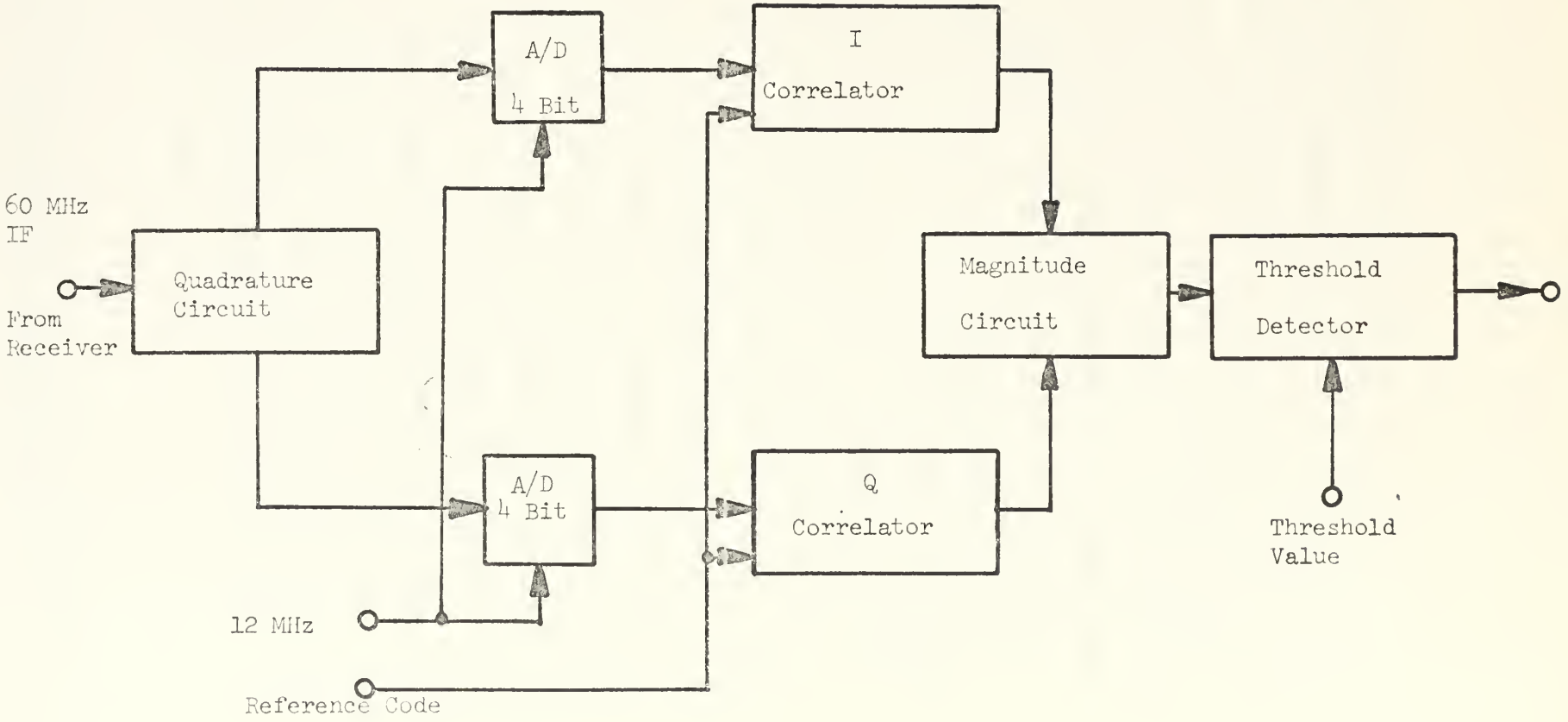

Figure 15. Correlation detector implementation

g. Discrete Analog Lignal Processing

Electrically Programmable Analog Transversal Filters are closely related to the concept of discrete analog signal processing (DASP), and the realization of Fourier transformers, matched filters and correlators, and adaptive filters. In DASP, analog data samples are stored, transferred, and operated upon by analog means, whereas in digital signal processing (DSP), digital or quantized samples are handled in binary logic. A major advantage of DSP is retained in DASP, namely, the precise transport delay, particularly in relation to coherent signal processing. An analog transversal filter constructed with reprogrammable, analog tap weights for DASP or also digital tap weights was recently reported.[9] It uses a multitapped CCD to provide the analog delay function and MNOS programmable non-volatile conductances as the analog weighted taps. Figure 16 shows a block diagram of an analog processor that provides Fourier Transform/Cross-Correlation to perform target identification functions. When N samples of the input signal are stored in the CCD delay line, the Fourier transform conductance matrix provides sin and cos weightings of these samples and forms N sums corresponding to the complex outputs of N/2 filters. The complex outputs are amplitude detected and correlated with the desired replica in the cross-correlation conductance matrix.

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[9] Lampe, D.R., and others, "An Electrically-Reprogrammable Analog Transversal Filter", ISSC Digest of Technical Papers, pp. 156-157, February 1974.

Adaptive filtering applications of these filters include voice recognition, adaptive equalization in MODEM's, remote intrusion detection, adaptive beam forming, etc.

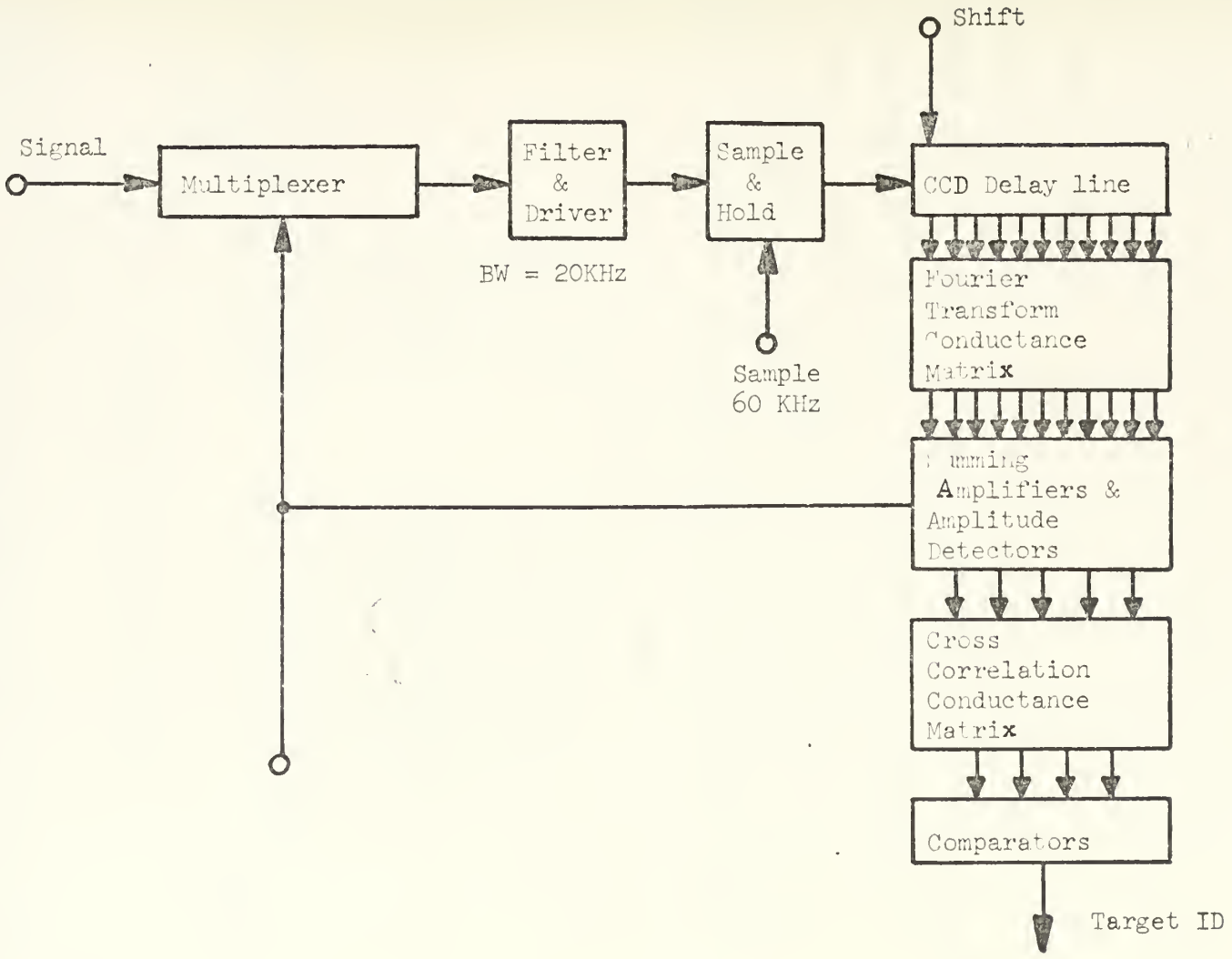

Figure 16. Transversal filter applications in DASP

3. Multiplexers

In the fields of communications, sonar, and radar, a large number of electronic systems depends on pulse multiplexing techniques to process sensor information to a more suitable and efficient format before transmission. CCD's parallel-to-serial capability permits simultaneous sampling of parallel signal channels with a single gate pulse, providing a new approach to time-division multiplexing in a integrated circuit format. The mode of operation of a CCD multiplexer is pulse amplitude modulation. A CCD multiplexer was demonstrated consisting in a simple variation on the CCD structure, which is a sampled-data analog delay line.[10] In the CCD multiplexer, inputs are applied to the delay line element positions, as depicted in Figure 17.

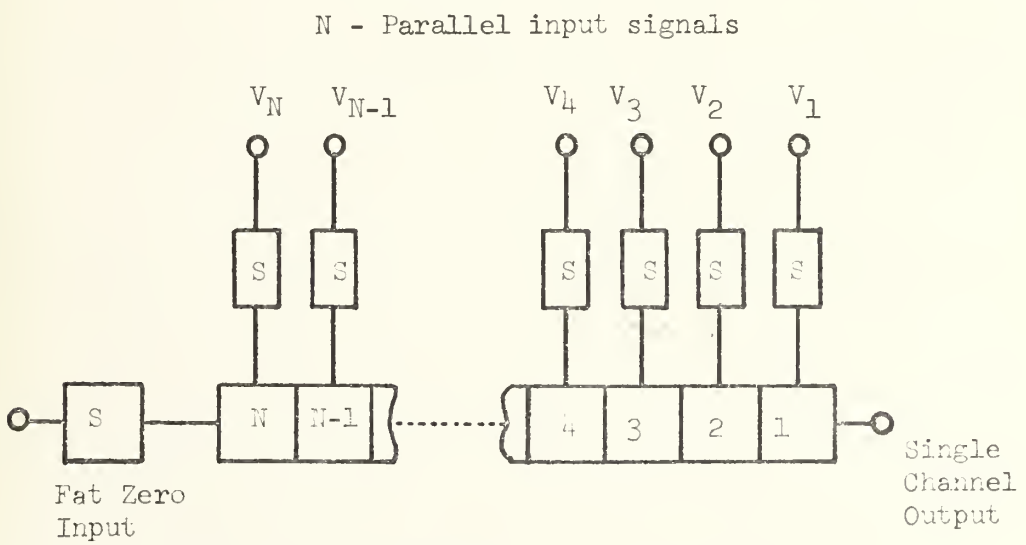

Figure 17. CCD Multiplexer Block Diagram

[10] Cheek, T.F., Jr., and others, "Design and Performance of Charge-Coupled Device Time-Division Analog Multiplexers", NELC CCD Applications Conference Proceedings, pp. 127-138, September 1973.

The sampled information is stored in the CCD as charge packets which are sequentially read out of the device by simple clock-controlled digital logic circuits.

C. STATE-OF-THE-ART

Since the introduction of the CCD and the BBD, there have been a number of proposed modifications to the basic structures in order to achieve specific performance goals. Some of these developments are described in this analysis, with emphasis on charge-coupled devices due to its large acceptance over bucket-brigade devices.

1. Fabrication

The CCD's initially constructed require three or more phase clocks to obtain the directionality of the signal flow. However, for most applications higher packing density and better performance may be achieved with two-phase charge-coupled structures. The asymmetrical potential wells or barriers in the surface potential, needed to provide the directionality of the information flow for the two-phase operation, can be achieved by incorporating one of the following features into the CCD structure:

1. Two thicknesses of the channel oxide.
2. DC offset voltage between two adjacent gates powered by the the same phase voltage.
3. Two levels of fixed charge in the channel oxide.
4. Ion implanted barriers.

The first three of the above can be implemented by self aligned, closely-spaced structures in the form of polysilicon gates overlapped by aluminum gates (overlapping gates technique); the fourth is achieved by ion implantation techniques. Overlapping gates and an improved ion implantation process are the currently most used fabrication techniques for two-phase CCD's. The important advantage

of the polysilicon-aluminum process is that it can be fabricated with very simple, conventional layout rules. The conductively connected charge-coupled device (C4D) is an improved version of the implanted barrier two-phase CCD. It is formed by providing self aligned, source-drain diffusions (or implants) between adjacent, refractory electrodes of a two-phase, ion implanted barrier CCD. These implants eliminate the inherently unstable exposed channel region presently found in CCD's with coplanar gates, without resorting to overlapping gates. The advantage of C4D's over polysilicon overlapping technique is that the parasitic loading between the clock lines on overlapping gates devices is eliminated in the ion implantation technique. However, C4D fabrication technique is quite complex and difficult to perform.

2. Transfer Modes

Charge transfer in CCD's can occur in two modes: surface and buried channel. Originally constructed CCD's operate by moving minority carriers along the surface of a semiconductor with voltage pulses applied to metal electrodes which are separated from the semiconductor by an insulating layer. The transit from one electrode to the next is determined by the minority carrier transport under the influence of their own potential, fringing fields, diffusion, and the trapping properties of interface states. Transport limitations are largely determined also by device geometry and surface state trapping. A modified structure was proposed in which the charges do not flow at the semiconductor surface; instead, they are confined to a channel which lies beneath the surface. This buried channel device has the

potential of eliminating surface state trapping; it offers the advantages of improved high-frequency response relative to surface devices because of strong fringe-field aided-transfer and also because carrier mobilities have higher values in bulk Si than in Si-SiO_2 interface. Further, the transfer efficiency should also be better at lower frequencies since surface state losses are eliminated. A special approach to buried-channel implementation was recently reported: the peristaltic charge-coupled device (PCCD). Based on the fact that the speed at which charge is transferred is mainly determined by the last fraction of each charge, the PCCD design forces that fraction of the charge to be located some distance away from the surface of the semiconductor, where charge carrier mobility is greater. In addition, these last charge fractions can be subjected to external drive fields, enabling the charge to be rapidly transferred to the neighboring element. The way in which the charge clouds (the last fraction in particular) are transported appears peristaltic in nature.

Two types of four-phase PCCD's have been demonstrated,[11] featuring transfer efficiency of 0.9998 to 0.99995 for real-zero operation and 0.9999 to 0.99995 for fat zero operation; the charge handling capacity is about 1.5 to 10^{11} to 3 X 10^{11} electrons cm^{-2}. Both types of CCD are expected to operate satisfactorily up to 1 GHz.

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[11] Esser, L.J.M., "The Peristaltic Charge-Coupled Device for High-Speed Charge Transfer", ISSSC Digest of Technical Papers, pp. 28-29, February 1974.

VIII. CONCLUSIONS

Based on the information which was provided in the previous sections, conclusions appear below by type of analog circuit. These conclusions are based on published design specifications and do not necessarily reflect actual performance of installed units.

A. ANALOG FUNCTION CIRCUITS

1. The continued push to smaller, better, higher-performance circuits at lower cost is turning current trend away from simple amplifiers, towards hybrids and monolithics functional IC's.

2. High performance obtained by new devices allows analog computations to be performed that would normally be done digitally, therefore, makes it possible to simplify many systems.

B. INTERFACING CIRCUITS

1. MOS technology is now beginning to appear in conversion circuits. These converters generally require smaller number of precision elements than comparable bipolar circuits. Inherent low power, noise immunity, lower external component cost, packing density, and high impedance level of MOS circuit allow the realization of high performance levels.

2. Monolithic trend is very strong in D/A converters up to 10-bit resolution.

C. CHARGE-TRANSFER DEVICES

1. Despite non-standard processing required, CCD's have significant performance advantages over BBD's and will probably dominate analog signal processing in the future.

2. Only commercially available CCD is used in imaging applications, not surveyed in this study.

D. GENERAL

1. A large move in linear IC fabrication is toward combination of technologies on the same chip. JFET's and MOSFET's processed on the same monolithic chip with bipolars will produce higher speeds and lower offsets.

2. Laser trimming and low-offset-current CMOS promise low cost, high-accuracy converters, multipliers, and log amps, each on a single chip.

3. Analog IC building blocks are readily available and have a very great application potential.

4. Developments in charge-transfer devices point to wider applicability in analog signal processing, but the extent of realized improvements in performance, true cost reductions and increased reliability is in doubt due to lack of quantitative data from user systems.

APPENDIX A

MANUFACTURERS INCLUDED IN THE SURVEY

The present survey is based on design specifications received from the following manufacturers:[12]

1. Analog Devices, Ind., Norwood, Mass
2. Analogic Corp., Wakefield, Mass.
3. Beckmann Instruments, Inc., Fullerton, Ca.
4. Burr Brown Research Corp., Tucson, Ariz.
5. Computer Labs, Inc., Greensboro, N.C.
6. Datel Systems, Inc., Canton, Mass.
7. ILC Data Device Corp., Hicksville, N.Y.
8. Dynamic Measurements Corp., Winchester, Mass.
9. Function Modules, Costa Mesa, Ca.
10. Harris Semiconductor, Melbourne, Fl.
11. Hybrid Systems Corp., Burlington, Mass.
12. HyComp, Inc., Maynard, Mass.
13. Intersil, Inc., Cupertino, Ca.
14. Intronics, Newton, Mass.
15. Micro Networks Corp., Worcester, Mass.
16. National Semiconductor Corp., Santa Clara, Ca.
17. Optical Electronics Inc., Tucson, Ariz.
18. Phoenix Data, Inc., Phoenix, Ariz.
19. Precision Monolithics, Inc., Santa Clara, Ca.
20. Teledyne Philbrick, Dedham, Mass.

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[12] Except for CTD's.

21. Zeltex, Inc., Concord, Ca.

Tables XII and XIII show, respectively, the number of models analyzed for each circuit and the participation of each manufacturer.

Table XII

Number of Models Analyzed in the Survey

Analog IC Circuit	No. Manufacturers	No. Models
Multipliers	8	73
Multifunction	3	8
Log Amps	6	26
A/D Converters	15	301
D/A Converters	18	421
Sample-Holds	12	51

Table XIII

Manufacturers Included in the Survey

	Analog Multipliers	Multi-Functions	Log and Log-Ratio Amps	A/D Converters	D/A Converters	Sample Holds
Analog Devices	28	4	4	19	23	6
Analogic	-	-	-	24	13	5
Beckmann	-	-	-	3	15	-
Burr Brown	13	1	1	14	19	7
Computer Labs	-	-	-	-	14	-
Datel	-	-	-	46	65	6
DDC	-	-	-	14	10	2
Dynamic Meas.	-	-	-	17	44	1
Function Modules	3	-	2	20	7	3
Harris Semicond.	-	-	-	-	-	1
Hybrid Systems	2	-	-	21	58	5
HyComp	-	-	-	-	6	-
Intersil	-	-	2	-	-	-
Intronics	17	3	-	-	2	-
Micro Networks	-	-	-	15	76	-
National Semicond.	-	-	-	-	-	5
Optical Electronics	3	-	10	5	6	8
Phoenix Data	-	-	-	77	5	-
Precision Monolithics	-	-	-	2	16	-
Teledyne Philbrick	4	-	7	14	27	1
Zeltex	2	-	-	10	15	2

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